ispXPGA™ Family

July 2002 — Advance Data Sheet

Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
- **High Logic Density for System-level Integration**
  - 139K to 1.25M system gates
  - 96 to 496 I/O
  - 1.8V, 2.5V, and 3.3V V_{CC} operation
  - Up to 414Kb sysMEM™ embedded memory
- **High Performance Programmable Function Unit (PFU)**
  - Four LUT-4 per PFU supports wide and narrow functions
  - Dual flip-flops per LUT-4 for extensive pipelining
  - Dedicated logic for adders, multipliers, multiplexers, and counters
- **Variable-Length Interconnect Routing Technology**
  - Optimum speed, power, and flexibility for logic interconnections
- **Flexible Memory Resources**
  - Multiple sysMEM Embedded RAM Blocks
    - Single port, Dual port, and FIFO operation
  - 64-bit distributed memory in each PFU
    - Single port, Double port, FIFO, and Shift Register operation
- **Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management**
  - True PLL technology
  - 6.255MHz to 320MHz operation
  - Clock multiplication and division
  - Phase adjustment
  - Shift clocks in 250ps steps
- **sysIO™ for High System Performance**
  - High speed memory support through SSTL and HSTL
  - Advanced buses supported through PCI, PCI-X, GTL+, LVDS, BLVDS, and LVPECL
  - Standard logic supported through LVTTL, LVCMOS 3.3, 2.5, and 1.8
  - Programmable drive strength for series termination
  - Programmable bus maintenance
  - sysHSI™ capability for ultra fast serial communications
    - Up to 850Mbps performance
    - Up to 20 channels per device
    - Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)
- **Flexible Programming, Reconfiguration, and Testing**
  - IEEE 1532 and 1149.1 compliant
  - Microprocessor configuration interface
  - Program E²CMOS while operating from SRAM

Table 1. ispXPGA Family Selection Guide

Family Member	System Gates	PFUs	LUT-4	Logic FFs	sysMEM Memory	Distributed Memory	sysHSI Channels	User I/O	Packaging	Body Size
ispXPGA 125	139K	484	1936	3.8K	92K	30K	4	176	256 fpBGA	17x17mm
									480 fpBGA[1]	35x35mm
									484 fpBGA	23x23mm
ispXPGA 200	210K	676	2704	5.4K	111K	43K	8	208	256 fpBGA	17x17mm
									480 fpBGA[1]	35x35mm
									484 fpBGA	23x23mm
ispXPGA 500	476K	1764	7056	14.1K	184K	112K	12	336	480 fpBGA[1]	35x35mm
									900 fpBGA	31x31mm
ispXPGA 1200	1.25M	3844	15376	30.7K	414K	246K	20	496	680 fpBGA[1]	40x40mm
									900 fpBGA	31x31mm

1. Thermally enhanced package.

ispXPGA Family Overview

The ispXPGA family of devices allows the creation of high-performance logic designs that are both non-volatile and infinitely re-programmable. Other FPGA solutions force a compromise being either re-programmable or non-volatile. This family couples this capability with a mainstream architecture containing the features required for today's system-level design.

Electrically Erasable CMOS (E^2CMOS) memory cells provide the ispXPGA family with non-volatile capability. These allow logic to be functional microseconds after power is applied, allowing easy interfacing in many applications. This capability also means that expensive external configuration memories are not required and that designs can be secured from unauthorized read back. Internal SRAM cells allow the device to be infinitely reconfigured if desired. Both the SRAM and E^2CMOS cells can be programmed and verified through the IEEE 1532 industry standard. Additionally, the SRAM cells can be configured and read-back through the sysCONFIG™ peripheral port.

The family spans the density and I/O range required for the majority of today's logic designs, 139K to 1.25M system gates and 96 to 496 I/O. The devices are available for operation from 1.8V, 2.5V, and 3.3V power supplies, providing easy integration into the overall system.

The system-level needs of designers are met through the incorporation of sysMEM dual-port memory blocks, sysIO advanced I/O support, and sysCLOCK Phase Locked Loops (PLLs). High-speed serial communications are supported through multiple sysHSI blocks, which provide clock data recovery (CDR) and serialization/de-serialization (SERDES).

The ispLEVER™ design tool from Lattice allows designers easy implementation of designs using the ispXPGA product. Synthesis library support is available for the major logic synthesis tools. The ispLEVER tool takes the output from these common synthesis packages and place and routes the design in the ispXPGA product. The tool allows floor planning and the management of other constraints within the device. The tool also provides outputs to common timing analysis tools for timing analysis.

To increase designer productivity, Lattice provides a variety of pre-designed modules referred to as IP cores for the ispXPGA product. These IP cores allow designers to concentrate on the unique portions of their design while using pre-designed block to implement standard functions such as bus-interfaces, standard communication-interfaces, and memory-controllers.

Through the use of advanced technology and innovative architecture the ispXPGA FPGA devices provide designers with excellent speed performance. Although design dependent, many typical designs can run at over 150MHz. Certain designs can run at over 300MHz. Table 2 details the performance of several building blocks commonly used by logic designers.

Table 2. ispXPGA Speed Performance for Typical Building Blocks

Function	Performance
64:1 Multiplexer	TBD
16:1 Multiplexer	TBD
16-bit adder	TBD
16x16 Pipelined Booth Multiplier	TBD
16 x 16 Asynchronous Booth Multiplier	TBD
32-bit up/down counter	TBD
32-bit Shift Register	TBD

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

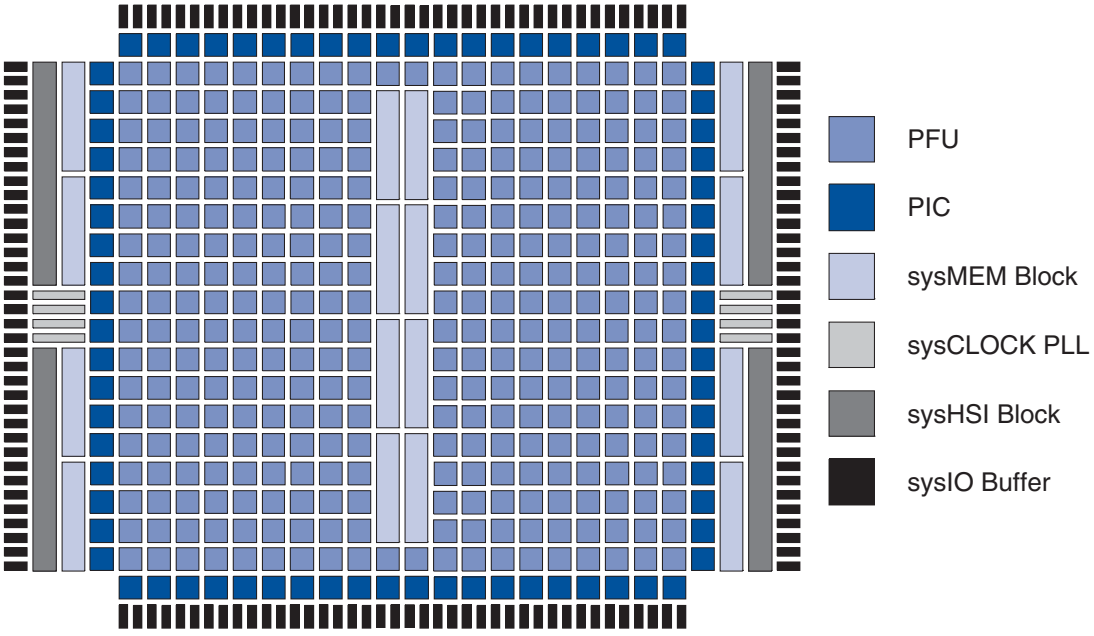
These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 850Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Figure 1. ispXPGA Block Diagram



Programmable Function Unit Description

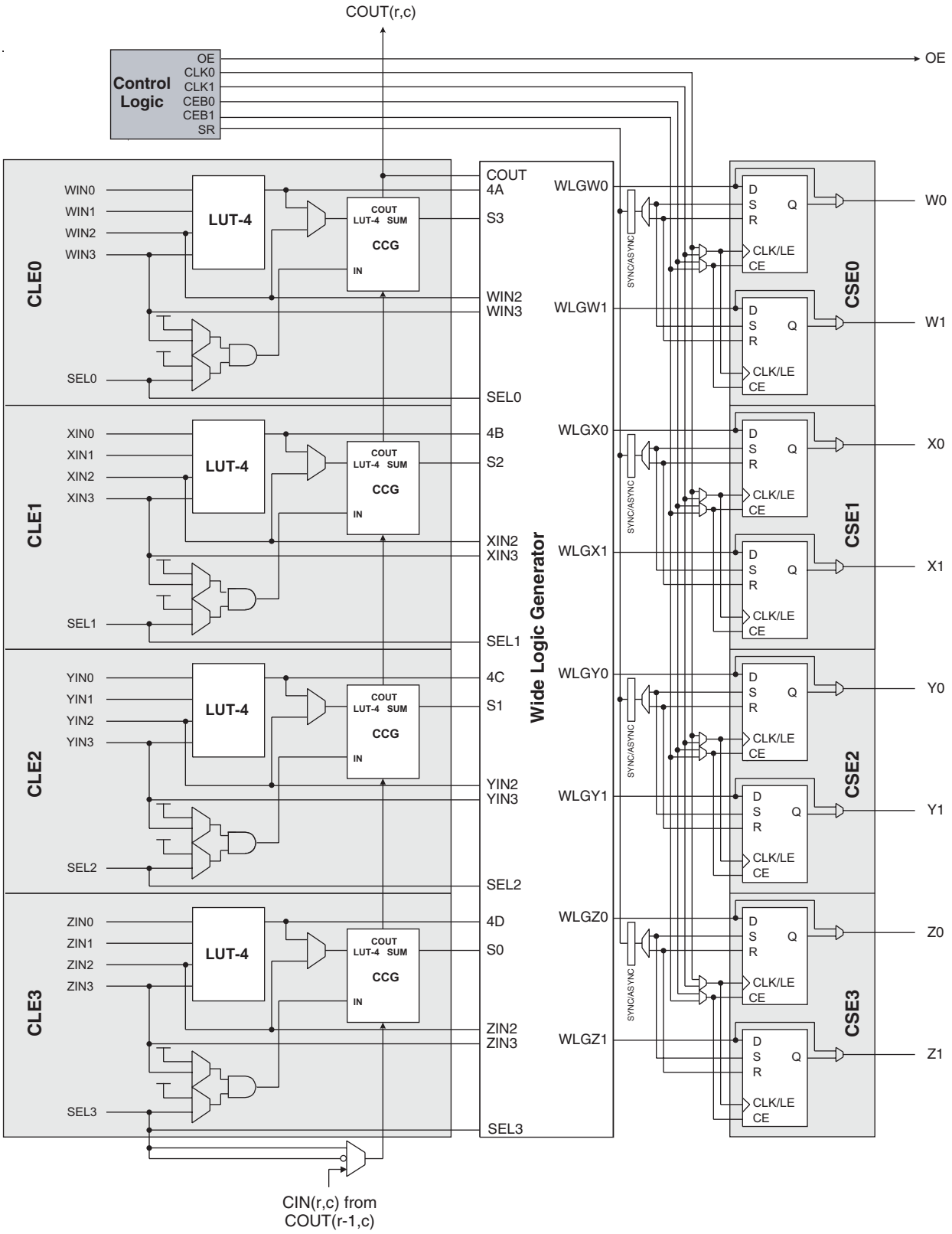
The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Figure 2. ispXPGA PFU



Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

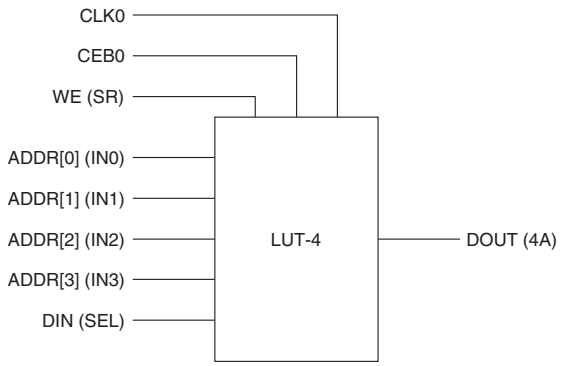
Look-Up Table - Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table - Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

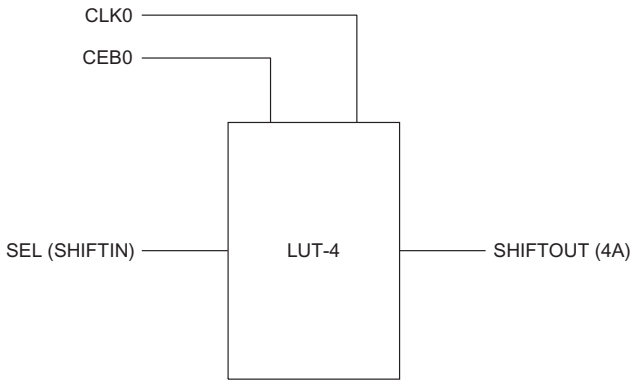
Figure 3. LUT in Distributed Memory Mode



Look-Up Table - Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

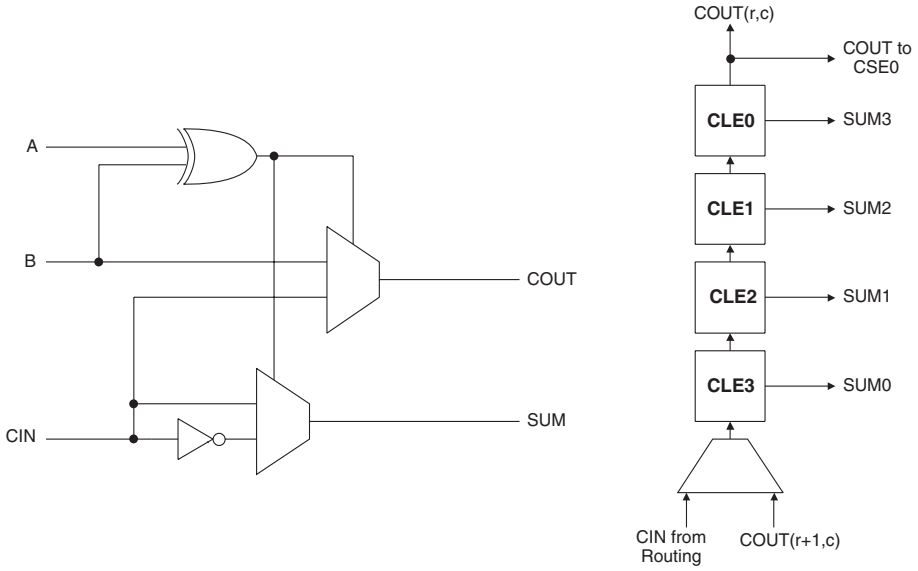
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

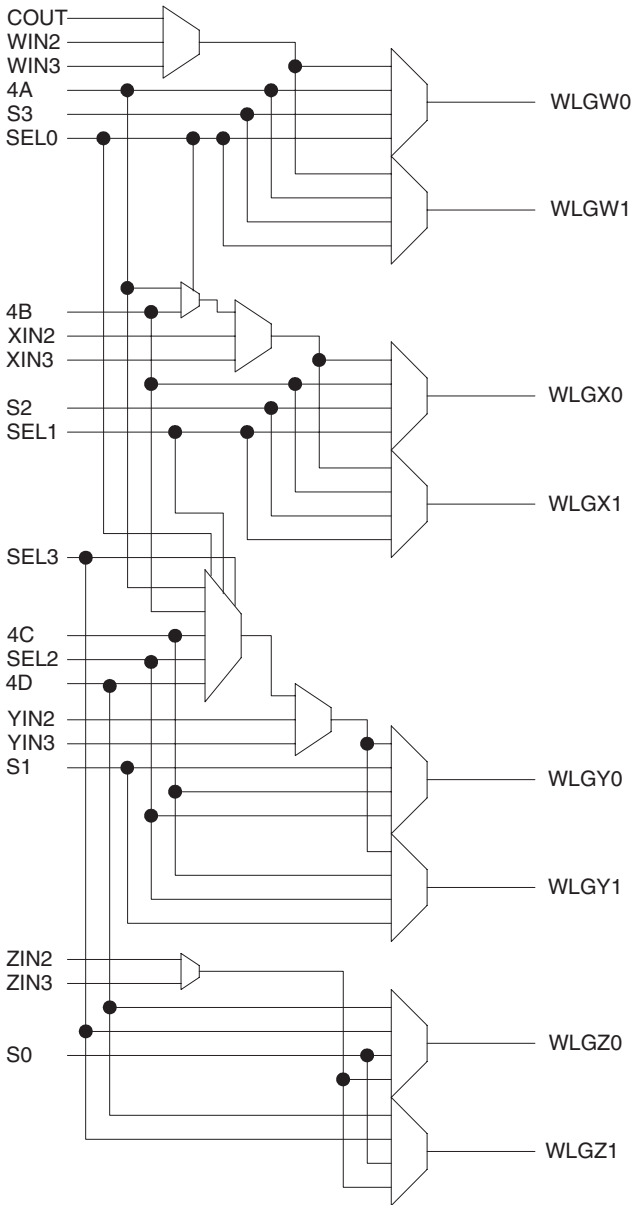
Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

Figure 6. ispXPGA Wide Logic Generator



Configurable Sequential Element

There are two registers in each CSE for a total of eight registers in each PFU. This high register count assists in implementing efficient pipelined applications with no utilization penalty. Each register can be configured as a latch or D type flip-flop with either synchronous or asynchronous set or reset. Figure 2 shows the signals that feed the register's D inputs. Feed-through signals in the architecture ensure that registers are efficiently utilized even if the accompanying LUT is occupied.

Control Logic

The control signals available to the registers in a PFU are Clock, Clock Enable, and Set/Reset. Figure 7 shows the various options available to generate the clock signal. As can be seen, the clock signal is the output of a 12:1 MUX with true and compliment versions available from the 12:1 MUX. Each CSE can chose whether it uses the true or compliment form of the clock. Figure 8 shows the Set/Reset selection for each PFU in the ispXPGA. A common

Set/Reset signal controls all the registers for each PFU. This common Set/Reset signal is composed of the logical OR term of the Global Set/Reset signal (GSR) and the selected signal from routing. The polarity of this signal is not controllable inside the PFU. Figure 9 shows the Clock Enable and Output Enable selection for each PFU.

Figure 7. Clock Selection per PFU

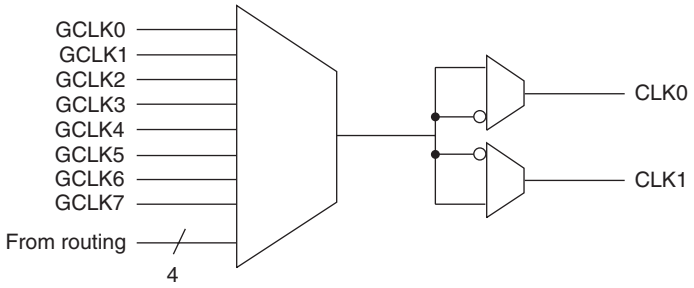


Figure 8. Set/Reset Selection per PFU

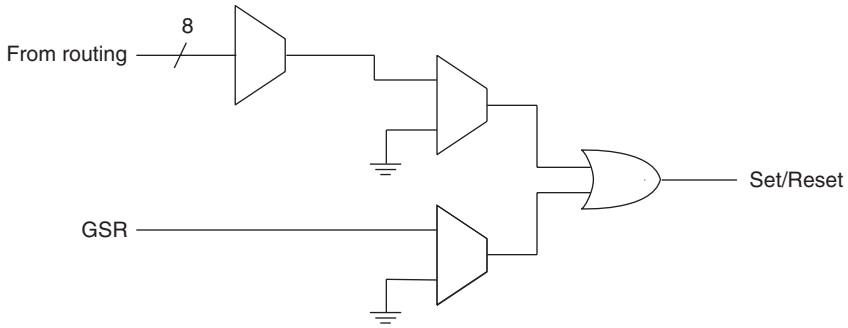
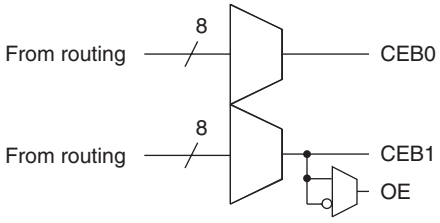


Figure 9. Clock Enable and Output Enable Selection per PFU

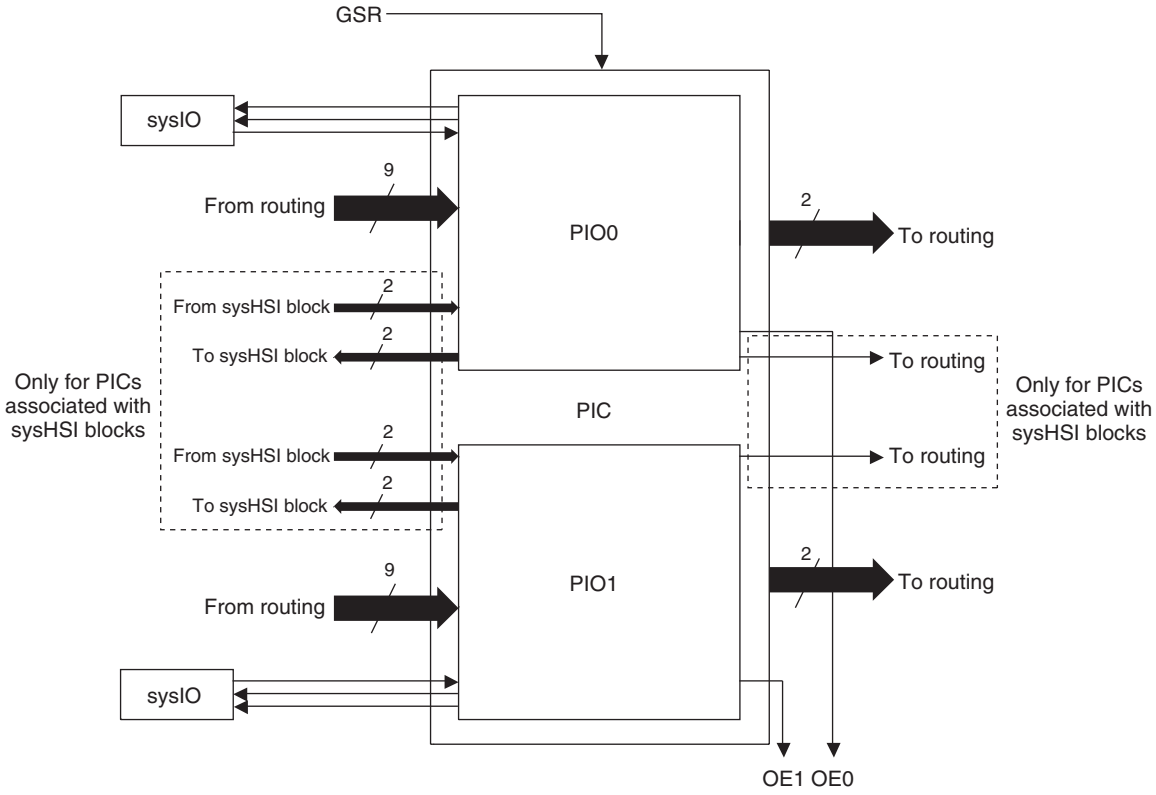


Programmable Input/Output Cell

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device.

Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. There are 18 inputs from routing, two inputs from the sysIO buffers, and the Global Set/Reset signal. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks. The four additional inputs come from the sysHSI block associated with the PIC. The four of the six additional outputs come from the PIC outputs and feed the sysHSI block, while the remaining two outputs feed routing. Figure 10 shows the block diagram of the PIC with the sysHSI block inputs and outputs.

Figure 10. ispXPGA PIC



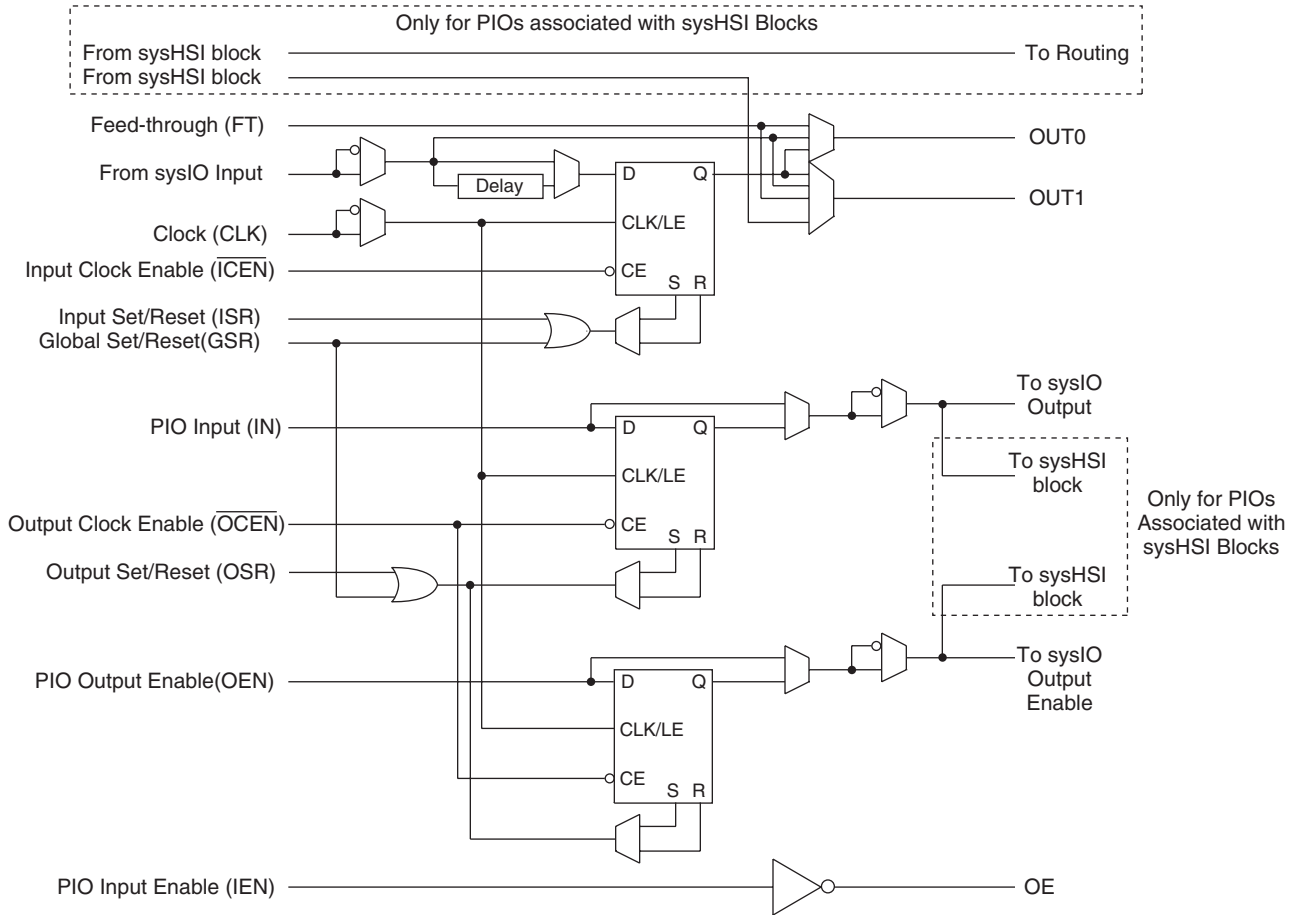
Programmable Input/Output

The PIO is the building block of a PIC. The PIO has a total of 11 inputs and five outputs. Nine of the 11 inputs are generated from routing. The inputs from routing are the PIO Input (IN), Feed-Thru (FT), Clock (CLK), Input Clock Enable (ICE), Input Set/Reset (ISR), Output Clock Enable (OCEN), Output Set/Reset (OSR), PIO Output Enable (OEN), and PIO Input Enable (IEN). The remaining inputs are the sysIO input buffer signal and the Global Set/Reset signal. Three of the five outputs (OUT0, OUT1, and OE) feed routing. The last two outputs feed the sysIO buffer directly as the output and output enable of the sysIO output buffer.

PIOs associated with sysHSI blocks contain two additional inputs and outputs to support the sysHSI block. The two inputs come from the sysHSI block associated with the PIO, and the two outputs feed the sysHSI block. One of the inputs routes directly through the PIO to routing, while the other is multiplexed with the Feed-Thru, register bypass, and Q output of the register to form the OUT1 output of the PIO. The outputs to the sysHSI block are the same signals as the outputs which feed the sysIO buffers (sysIO Output and sysIO Output Enable).

Each PIO has an input register, an output register, and an output enable register as shown in Figure 11. The input register path of the PIO has a ‘delay’ option, which slows the data-flow. A two-input OR function of the Global Set/Reset (GSR) and Set/Reset (ISR or OSR) signals creates the set/reset term for the respective registers. Each PIO has two pairs of set/reset and clock enable signals. One is exclusive to the input register, whereas the other is common for both the output and output enable registers. The clock (CLK) is common to all registers in a PIO, and the polarity of the clock is controllable. The input, output, and the output enable registers can be configured as a latch or D-type flip-flop. Each PIO is capable of generating an output enable signal, which in turn becomes a PIC output.

Figure 11. ispXPGA PIO



VLI Routing Resources

The ispXPGA architecture contains a Variable-Length-Interconnect (VLI) routing technology connecting the PFUs, PICs, and EBRs in the device. There are four types of routing resources, Global Lines, Long Lines, General Interconnect, and Local Lines forming the global routing structure. This allows a signal to be routed to any element in the device with the optimal delay.

The Global Lines consist of global clock lines and a global set/reset line. These lines are routed to all elements in the device. They are specifically designed for high speed, predictable timing regardless of fan-out. The global clock lines can also be used as dedicated inputs.

The Long Lines consist of Horizontal and Vertical Long Lines (HLL and VLL). The VLL and HLL are tri-statable lines spanning the entire device. These lines allow fast routing for high fan-out nets and general-purpose functions.

The General Interconnect consists of Double and Deca Lines. The Double Lines connect up to three elements (two plus the driving element), while the Deca Lines connect up to eleven elements (ten plus the driving element).

The Local Lines are extremely fast routing paths consisting of Feedback and Direct Connect Lines. The Feedback Lines are internal routing paths from the PFU outputs to the PFU inputs. The Direct Connect Lines connect all adjacent elements.

The Common Interface Block (CIB) provides the link between the logic element (PFU, PIC, or EBR) and the VLI Routing resources. The CIB is a switch matrix that can be programmed to connect virtually any routing resource to any input or output of the logic element.

Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs (see Look-Up Table -Distributed Memory Mode in the PFU section above). Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM blocks. Refer to Table 1 for memory resources per device.

sysMEM Blocks

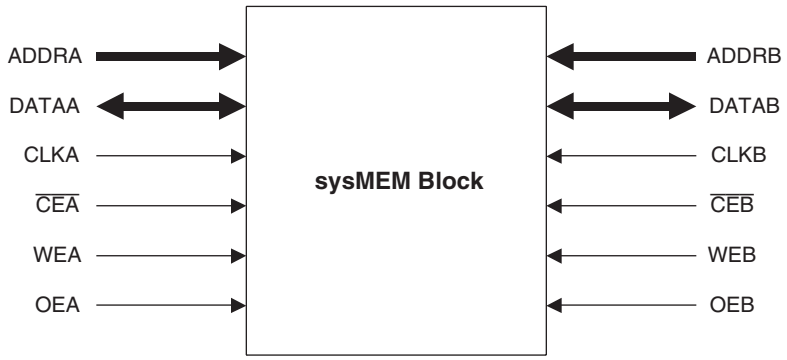
The sysMEM blocks are organized in columns distributed throughout the device. Each EBR contains 4.6K bits of dual-port RAM with dedicated control, address, and data lines for each port. Each column of sysMEM blocks has dedicated address and control lines that can be used by each block separately or cascaded to form larger memory elements. The memory cells are symmetrical and contain two sets of identical control signals. Each port has a read/write clock, clock enable, write enable, and output enable. Figure 12 illustrates the sysMEM block.

The ispXPGA memory block can operate as single-port or dual-port RAM. Supported configurations are:

- 512 x 9 bits single-port (8 bits data / 1 bit parity)
- 256 x 18 bits single-port (16 bits data / 2 bits parity)
- 512 x 9 bits dual-port (8 bits data / 1 bit parity)
- 256 x18 bits dual-port (16 bits data / 2 bits parity)

The data widths of “9” and “18” are ideal for applications where parity is necessary. This allows 9 data bits, 8 data bits plus a parity bit, 18 data bits, or 16 data bits plus two parity bits. The logic for generating and checking the parity must be customized separately.

Figure 12. sysMEM Block Diagram

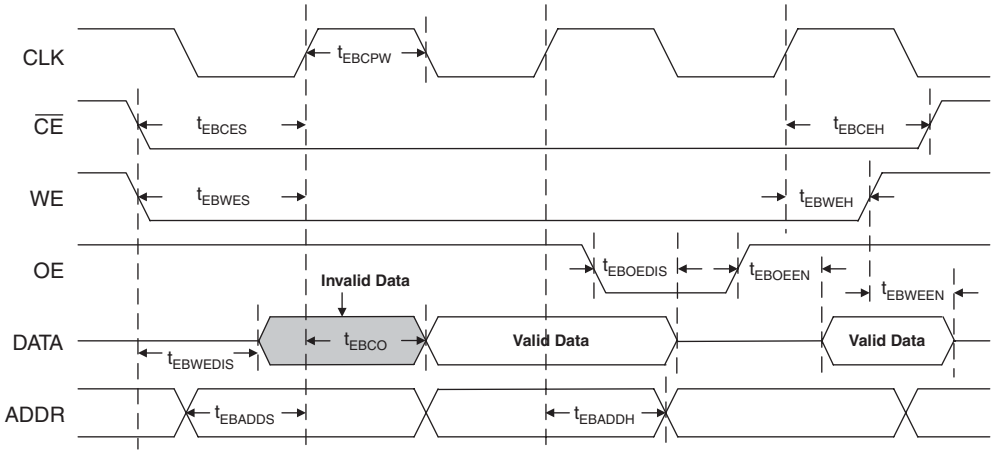


Read and Write Operations

The ispXPGA EBR has fully synchronous read and write operations as well as an asynchronous read operation. These operations allow several different types of memory to be implemented in the device.

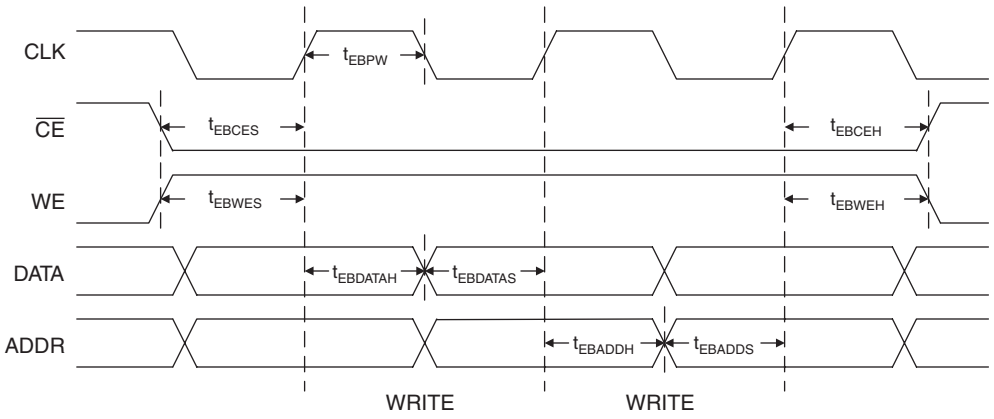
Synchronous Read: The Clock Enable ($\overline{CE}$) and Write Enable (WE) signals control the synchronous read operation. When the $\overline{CE}$ signal is low, the clock is enabled. When the WE signal is low the read operation begins. Once the address (ADDR) is present, a rising clock edge (or falling edge depending on polarity) causes the stored data to be available on the DATA port. Figure 13 illustrates the synchronous read timing.

Figure 13. EBR Synchronous Read Timing Diagram



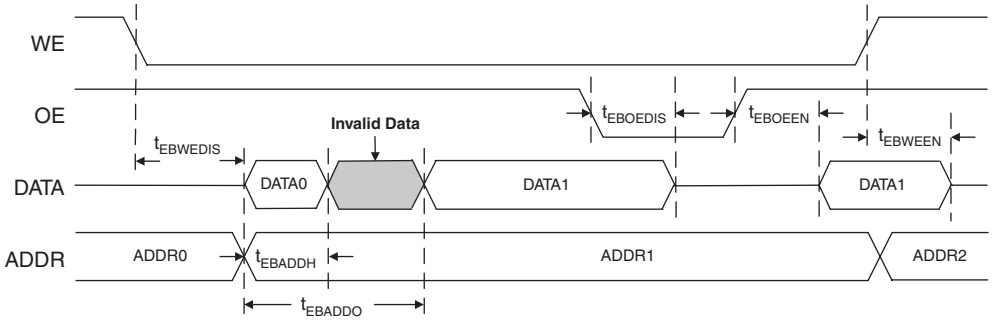
Synchronous Write: The $\overline{CE}$ and WE signals control the synchronous write operation. When the $\overline{CE}$ signal is low, the clock is enables. When the WE signal is high and the write operation begins. Once the address and data are present and the Output Enable (OE) is active, a rising clock edge (or falling edge depending on polarity) causes the data to be stored into the EBR. Figure 14 illustrates the synchronous write timing.

Figure 14. EBR Synchronous Write Timing Diagram



Asynchronous Read: The WE signal controls the asynchronous read operation. When the WE signal is low, the read operation begins. Shortly after the address is present, the stored data is available on the DATA port. Figure 15 illustrates the asynchronous read timing. For more information about the EBR, refer to Lattice technical note number TNXXXX *ispXPGA sysMEM Memory Usage and Design Guidelines,* available at www.latticesemi.com.

Figure 15. EBR Asynchronous Read Timing Diagram



sysCLOCK PLL Description

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset, and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are aligned either at the board level or the device level.

The ispXPGA devices provide up to eight PLLs. Each PLL receives its input clock from its associated global clock pin, and its output is routed to the associated global clock net. For example, PLL0 receives its clock input from the GCLK0 global clock pin and provides output to the CLK0 global clock net. The PLL also has the ability to output a secondary clock that is a division of the primary clock output. When using the secondary clock, the secondary clock will be routed to the neighboring global clock net. For example, PLL0 will drive its primary clock output on the CLK0 global clock net and its secondary clock output will drive the CLK1 global clock net. Additionally, each PLL has a set of PLL_RST, PLL_FBK, and PLL_LOCK signals. The PLL_RST signal can be generated through routing or a dedicated dual-function I/O pin. The PLL_FBK signal can be generated through a dedicated dual-function I/O pin or internally from the Global Clock net associated with the PLL. The PLL_LOCK signal feeds routing directly from the sysCLOCK PLL circuit. Figure 17 illustrates how the PLL_RST and PLL_FBK signals are generated.

Each PLL has four dividers associated with it, M, N, V, and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The V divider allows the VCO frequency to operate at higher frequencies than the clock output, thereby increasing the frequency range. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to the adjacent global clock net. Different combinations of these dividers allow the user to synthesize clock frequencies. Figure 16 shows the ispXPGA PLL block diagram.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines of the PLL. For more information on the PLL, please refer to Lattice technical note number TN1003, *sysCLOCK PLL Usage and Design Guidelines,* available at www.latticesemi.com.

Figure 16. ispXPGA PLL Block Diagram

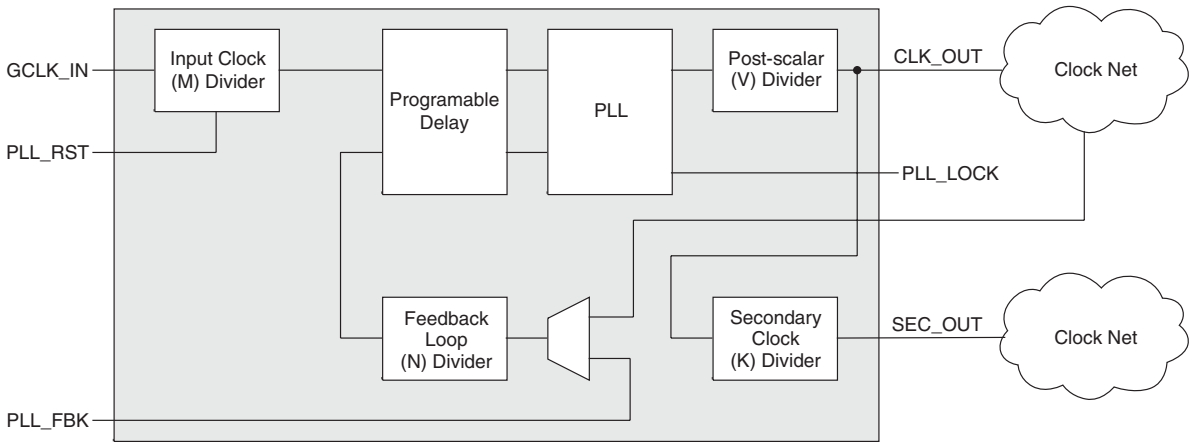
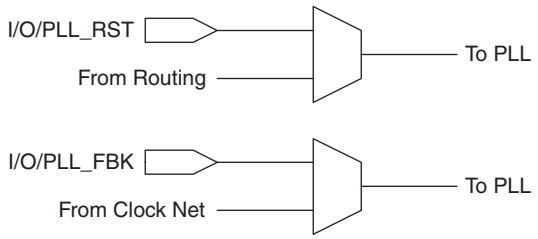


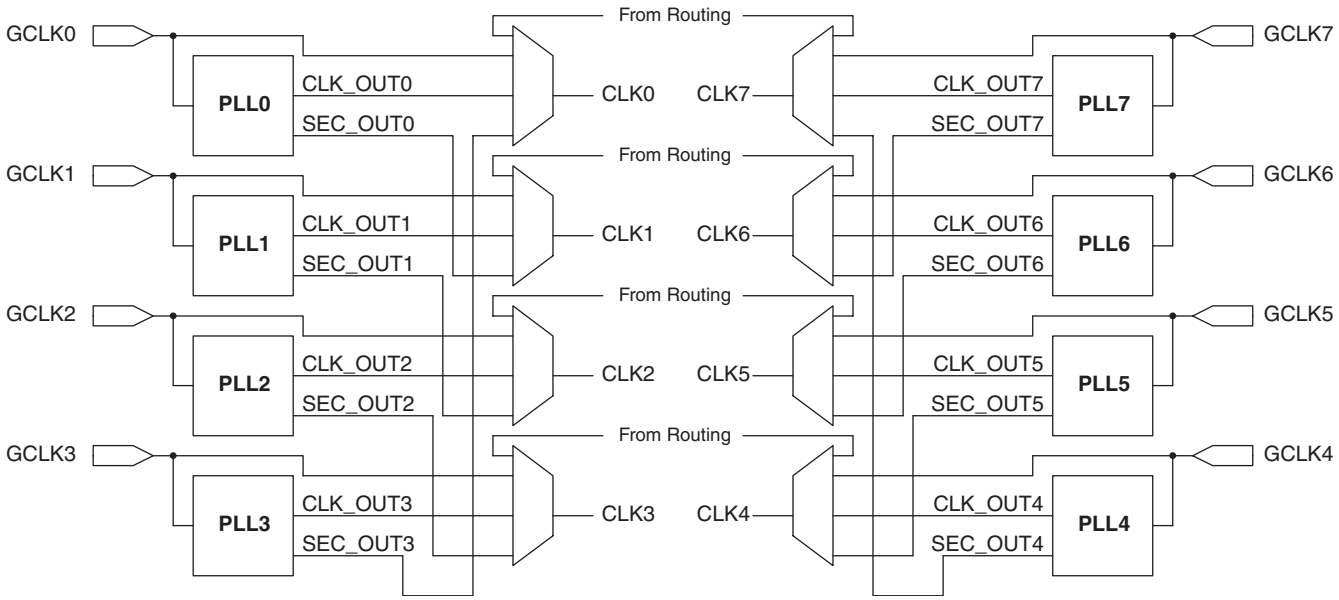
Figure 17. ispXPGA PLL_RST and PLL_FBK Generation



Clock Routing

The Global Clock Lines (GCLK) have two sources, their dedicated pins and the sysCLOCK circuit. Figure 18 illustrates the generation of the Global Clock Lines.

Figure 18. Global Clock Line Generation



sysIO Capability

The ispXPGA devices are divided into as many as eight sysIO banks, where each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O is individually configurable based on the bank's V_{CCO} and V_{REF} settings. In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down, or a bus-keeper latch.

Table 5 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

The TOE, CFG0, and IEEE 1149.1 TAP pins of the ispXPGA device are the only pins that do not have the sysIO capabilities. The TOE and CFG0 pins operate off the V_{CC} of the device, supporting only the LVCMOS standard corresponding to the device supply voltage. The TAP pins have a separate supply voltage (V_{CCJ}), which determines the LVCMOS standard corresponding to that supply voltage.

There are three classes of I/O interface standards that are implemented in the ispXPGA devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V, and 3.3V LVCMOS interface standards. Additionally, PCI, PCI-X, and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, and GTL+. Usage of these particular I/O interfaces requires an additional V_{REF} signal. At the system level a termination voltage, V_{TT}, is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The third type of interface standards are the differential standards LVDS, BLVDS, and LVPECL. The differential standards require two I/O pins to create the differential pair. The logic level is determined by the difference in the two signals. Table 4 lists how these interface standards are implemented in the ispXPGA devices.

For more information on sysIO capability, refer to Lattice technical note number TN1000, *sysIO Usage Guidelines for Lattice Devices* available at www.latticesemi.com.

Table 4. Differential Interface Standard Support

		sysIO Buffer Not Using sysHSI Block	sysIO Buffer Using sysHSI Block
LVDS	Driver	Not Supported	Supported
	Receiver	Not Supported	Supported
BLVDS	Driver	Supported by Using External Resistors	Not Supported
	Receiver	Supported	Supported
LVPECL	Driver	Supported by Using External Resistors	Not Supported
	Receiver	Supported	Supported by Using External Resistors

Table 5. ispXPGA Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI	3.3V	N/A	N/A
PCI-X	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I, II	3.3V	1.5V	1.5V
SSTL2, Class I, II	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
HSTL, Class IV	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL	3.3V	N/A	N/A
LVDS[1]	2.5V/3.3V	N/A	N/A
BLVDS	2.5V/3.3V	N/A	N/A

1. V_{CCO} must be 2.5V for high speed serial operations (sysHSI block).

High Speed Serial Interface Block (sysHSI Block)

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispXPGA devices have multiple sysHSI blocks.

Each sysHSI block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in sysHSI blocks share a common clock and must operate at the same nominal frequency. Figure 19 shows the sysHSI block.

Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI technical notes). The encoding and decoding of the 10B/12B standard are performed within the device. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the sysHSI block.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI blocks can be grouped together to form a source synchronous interface of 1-10 channels.

Table 6 shows the clock sources available for the REFCLKs of the different sysHSI blocks. The Signal Description table in this data sheet provides the descriptions of the sysHSI block inputs and outputs.

For more information on the SERDES/CDR, refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

Figure 19. sysHSI Block Diagram

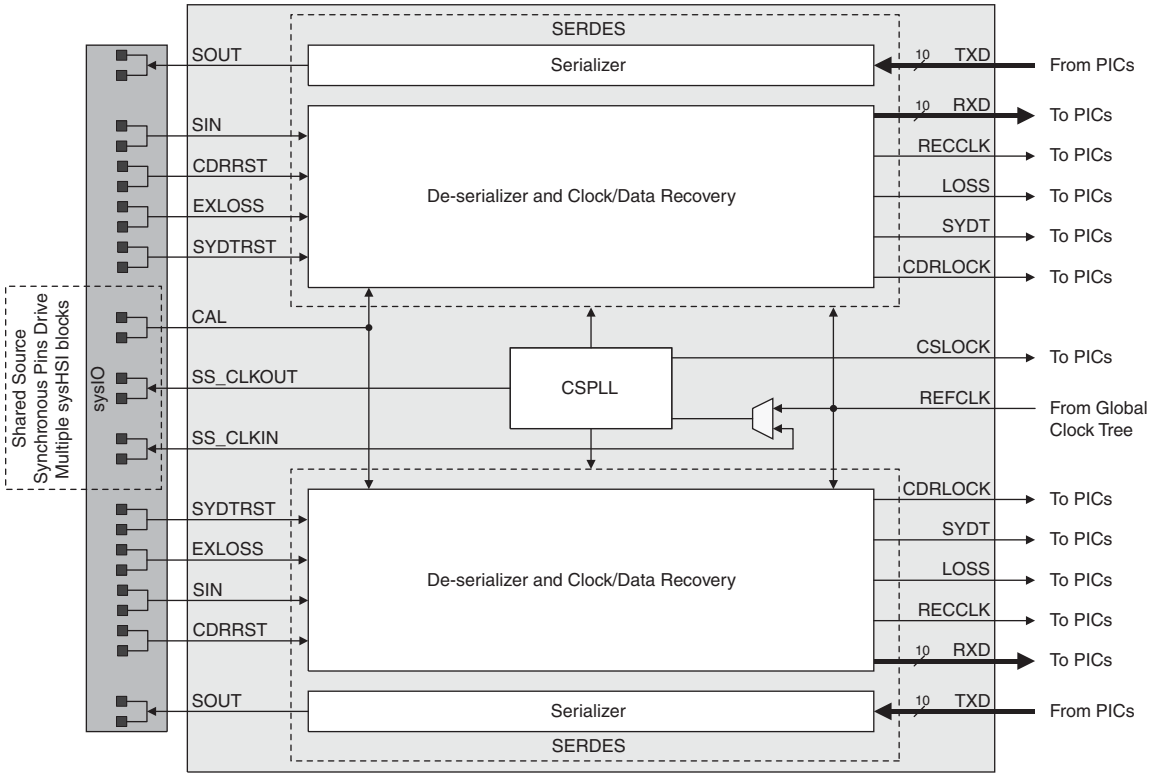


Table 6. sysHSI Block REFCLK Selections[1]

sysHSI Block	Available Global Clock Nets
0	GCLK0, GCLK1, GCLK2, GCLK3
1	GCLK0, GCLK1, GCLK2, GCLK4
2	GCLK0, GCLK1, GCLK2, GCLK5
3	GCLK0, GCLK1, GCLK3, GCLK6
4	GCLK0, GCLK1, GCLK3, GCLK7
5	GCLK0, GCLK3, GCLK5, GCLK7
6	GCLK0, GCLK2, GCLK5, GCLK7
7	GCLK0, GCLK1, GCLK5, GCLK6
8	GCLK0, GCLK5, GCLK6
9	GCLK0, GCLK5, GCLK6, GCLK7

1. Table 6 applies to all devices. Ignore sysHSI blocks not available in a specific device.

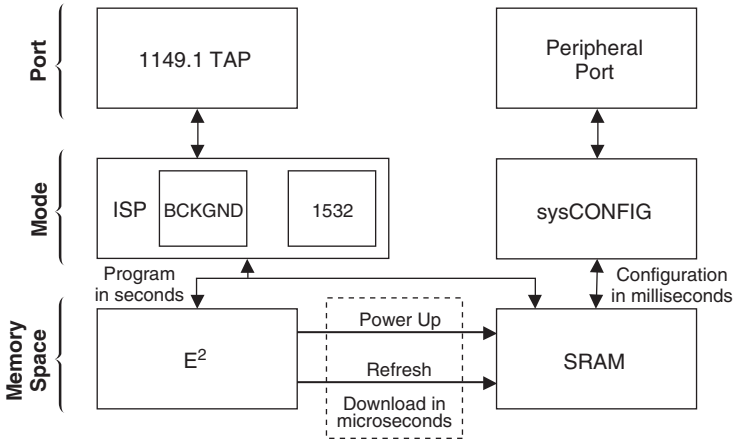
Configuration and Programming

The ispXPGA family of devices takes a unique approach to FPGA configuration memory. It contains two types of memory, Static RAM and non-volatile E^2CMOS cells. The static RAM is used to control the functionality of the device during normal operation and the E^2CMOS memory cells are used to load the SRAM. The E^2CMOS memory module can be thought of as the hard drive for the ispXPGA configuration and the SRAM as the working configuration memory. There is a one-to-one relationship between SRAM memory and the E^2CMOS cells. The SRAM is configured either from the E^2CMOS memory or from an external source, as shown in Figure 20.

Figure 20 shows the different ports and modes that are used in the configuration and programming of the ispXPGA devices. There are two possible ports that can be used for configuration of the SRAM memory; the IEEE Std. 1149.1 Test Access Port (TAP), which accommodates bit-wide configuration and the Peripheral port, which allows byte-wide configuration. When programming the E^2CMOS memory, only the 1149.1 TAP can be used.

Configuration and programming done through the 1149.1 Test Access Port (TAP) are fully compliant to both the IEEE Std. 1149.1 Boundary Scan TAP specification and the IEEE Std. 1532 In-System Configuration specification. To configure or program the device using the 1149.1 TAP the device must be in the ISP mode. To configure the SRAM memory using the Peripheral Port, the device must be in the sysCONFIG mode. Upon power-up, the device's SRAM memory can be configured either from the E^2CMOS memory or from an external source through the sysCONFIG mode. Additionally, the SRAM can be re-configured from the E^2CMOS memory by executing a "REFRESH." See Lattice technical note number TN1026, *sysCONFIG Usage Guide,* for more in depth information on the different programming modes, timing and applications, available at www.latticesemi.com.

Figure 20. Dual Memory Program and Configuration



Configuration/Programming Pins

The pins used for ISP Mode and sysCONFIG Mode and the associated attributes are summarized in Table 7. Some pins have programmable attributes that can be set in the design software to control different characteristics of the pin. These attributes are listed in the "Attribute" column of Table 7. Pins that can have an attribute of "PULL" have the option of having an active pull-up rather than being open-drain.

Many of the pins described in Table 7 are dedicated for programming and configuration and have no other functions. Included in this group of pins are the 1149.1 TAP pins and any of the pins used for the "REFRESH" mode. The remainder of the pins used for the sysCONFIG mode have the option of being PERSISTENT where the pin continues to function as a configuration pin during normal operation of the device. If a pin is PERSISTENT the design software will not allow that pin to be used for any logic or other function other than configuration.

Refer to the Lattice *sysCONFIG Usage Guide* for a full description of the pins used for both configuration and programming.

Table 7. Configuration Pins

Pin	Direction	Attribute	Characteristic	Mode Used
CFG0	Input	—	Pull-up	ISP/REFRESH/sysCONFIG
$\overline{\text{PROGRAM}}$	Input	—	Pull-up	ISP/REFRESH/sysCONFIG
DONE	Bi-directional	PULL	Open-Drain	ISP/REFRESH/sysCONFIG
TDI	Input	—	Pull-up	ISP
TCK	Input	—	—	ISP
TDO	Output	—	Pull-up	ISP
TMS	Input	—	Pull-up	ISP
$\overline{\text{INIT}}$	Bi-directional	PERSISTENT	Open-Drain	sysCONFIG
READ	Input	PERSISTENT	—	sysCONFIG
CCLK	Input	PERSISTENT	—	sysCONFIG
$\overline{\text{CS}}$	Input	PERSISTENT	—	sysCONFIG
D[0:7]	Bi-directional	PERSISTENT	—	sysCONFIG

Configuration/Programming Modes

The CFG0 pin, as shown in Table 8, selects the port used to configure the SRAM memory. To configure the SRAM memory from the E^2CMOS memory, either at power-up or when using the REFRESH command, the CFG0 pin must be held high. To configure the SRAM from an external source using the Peripheral Port, CFG0 must be driven to a logic '0.'

There are two modes that can be used to program the E²CMOS memory. These are the IEEE 1532 compliant mode and the Background programming mode. When programming using the 1532 mode, the device I/Os are controlled by the 1149.1 boundary scan register and the internal logic is disabled. Programming using the Background programming mode allows the device to continue operation and the I/Os are driven by the core logic rather than by the boundary scan register. The SRAM memory can only be configured in 1532 mode when using the 1149.1 TAP for configuration. Readback of the SRAM memory can be done in a Background mode, allowing the device to remain active.

Both the SRAM and the E²CMOS memory are configurable at any time through the 1149.1 TAP using ISP mode. When configuring the SRAM through the Peripheral Port using the sysCONFIG mode, it is strongly recommended against configuring or programming the device using the 1149.1 TAP. Additionally, boundary scan tests should not be executed until all configuration operations have completed.

Table 8. Configuration Pin Selection

Memory	CFG0	Mode Implemented	Configuration/Programming Port
SRAM	0	sysCONFIG	Configure from Peripheral Port
SRAM	1[1]	ISP or Refresh	Configure from E²CMOS Cells or 1149.1 TAP
E²	X[1]	ISP	Program from 1149.1 TAP

1. ISP Mode is always available regardless of the CFG0 state. However, ISP Mode operations are not recommended when sysCONFIG is active.

SRAM Refresh Operation

The SRAM can be refreshed at any time from the E²CMOS memory. This is the fastest way to configure the SRAM. With the CFG0 pin held high, the $\overline{\text{PROGRAM}}$ pin is toggled and held low for a minimum of $t_{REFRESH}$. The I/O pins will tristate during the re-configuration process and the internal DONE bit will clear. Driving the $\overline{\text{PROGRAM}}$ pin high will initiate the download of the configuration from the E²CMOS memory to the SRAM and initiate the wake-up process.

sysCONFIG Configuration

Next to configuring the memory from the E²CMOS memory the sysCONFIG Mode is the fastest way to configure the device. By using the 8-bit data port, reading and writing to the configuration SRAM can be done directly by a host device without having to program and download from the E²CMOS Cells. The host device must provide the following signals to the device: D0 through D7, CCLK, $\overline{\text{CS}}$, $\overline{\text{PROGRAM}}$ and READ.

Persistent Programming Pins

Many of the programming pins used when in sysCONFIG Mode are dual-purpose pins. When the $\overline{\text{PROGRAM}}$ pin is driven low, the dual-purpose pins become dedicated programming pins. The designer can choose if the dual-purpose pins become dedicated programming pins by setting the Persistent attribute in the software (Table 7). The Persistent attribute can be set in the design software in the constraint manager. To make a persistent pin a dedicated programming pin, set the Persistent attribute to ON. For more information on hardware attributes, please see the design software help notes.

Write to SRAM

To write data to the SRAM from the host device, the $\overline{\text{PROGRAM}}$ pin must be driven low for a minimum of t_{PRGM}. The I/Os will be tri-stated and the peripheral configuration pins take over control of the configuration process. The DONE Bit will be cleared and the DONE pin will be driven low. The $\overline{\text{INIT}}$ pin will be set low while the device is transitioning to the Configuration Mode. When the $\overline{\text{INIT}}$ pin goes high, the ispXPGA device is ready for programming.

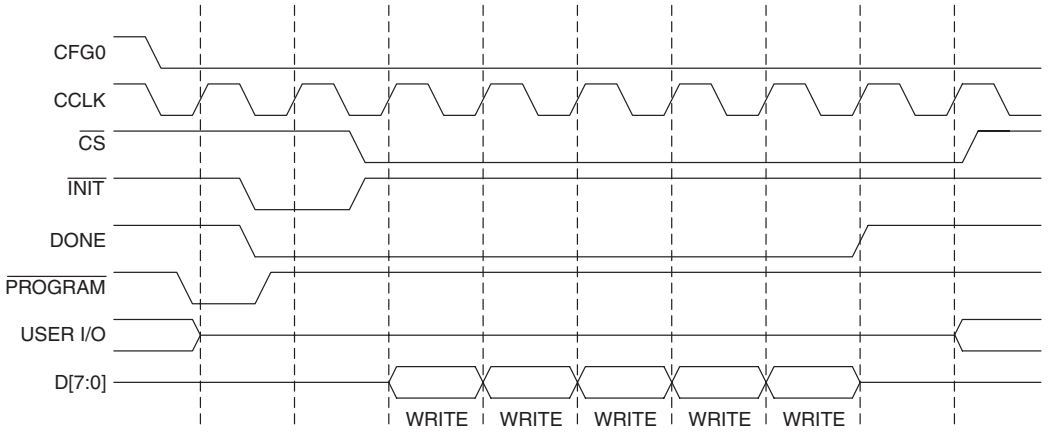
The configuration process will begin when the host drives the $\overline{\text{CS}}$ signal low and starts CCLK. Data will be read in on the rising edge of CCLK one byte at a time. If the host needs to pause, it will drive $\overline{\text{CS}}$ high until it is ready to continue. Once the data stream is complete, the CRC will have calculated if an error occurred. If an error happened during the write process, ispXPGA will drive the $\overline{\text{INIT}}$ pin low. If no error occurred, the $\overline{\text{INIT}}$ pin will remain pulled high. After the CRC passes, the DONE Bit will be set which will then drive the DONE pin high and the wake-up pro-

cess will begin. Timing for the writing to the SRAM is shown in Figure 21. Figure 22 shows the flow for writing data to the device SRAM.

Table 9. ISP Instructions

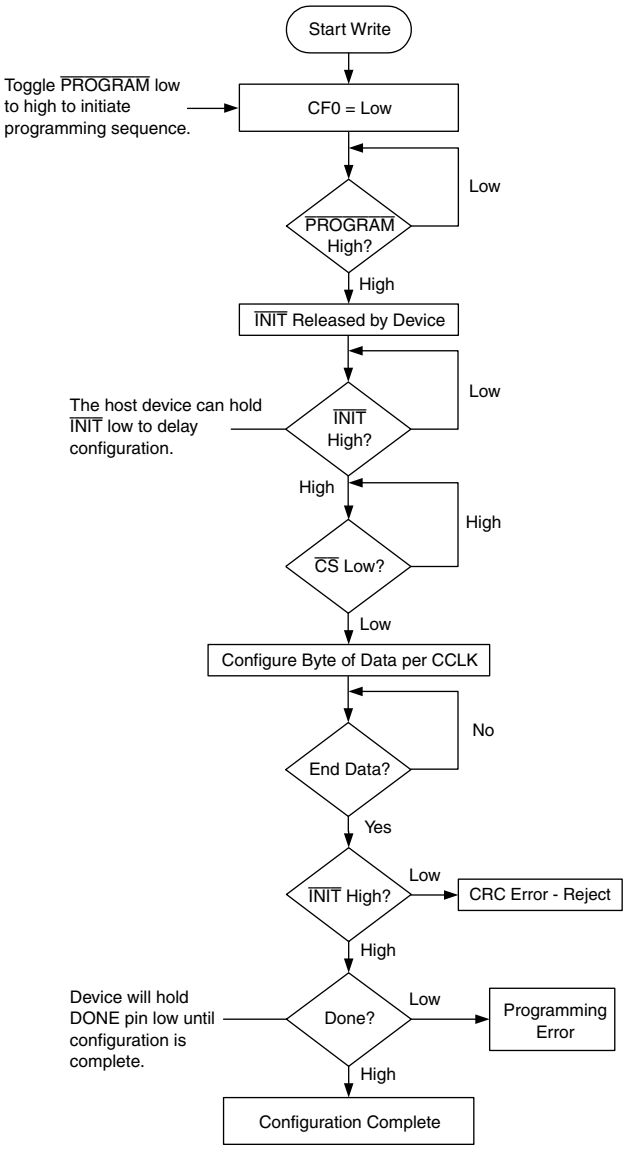
ISP Instruction	Memory	ISC 1532 Compliant	BSCAN Register Control
Standby Programming	E^2	Yes	Yes
Transparent Programming	E^2	No	No
Direct Configuration	SRAM	Yes	Yes
Transparent Read	SRAM	No	No

Figure 21. SRAM Write Cycle Timing Diagram



Note: Total SRAM Write Cycle does not occur in five clock cycles.

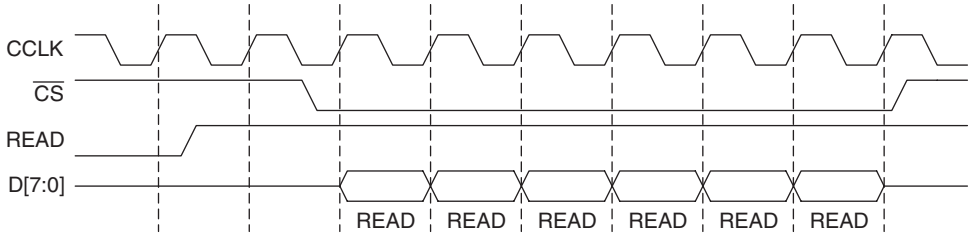
Figure 22. SRAM Write Cycle Flowchart



Read from SRAM

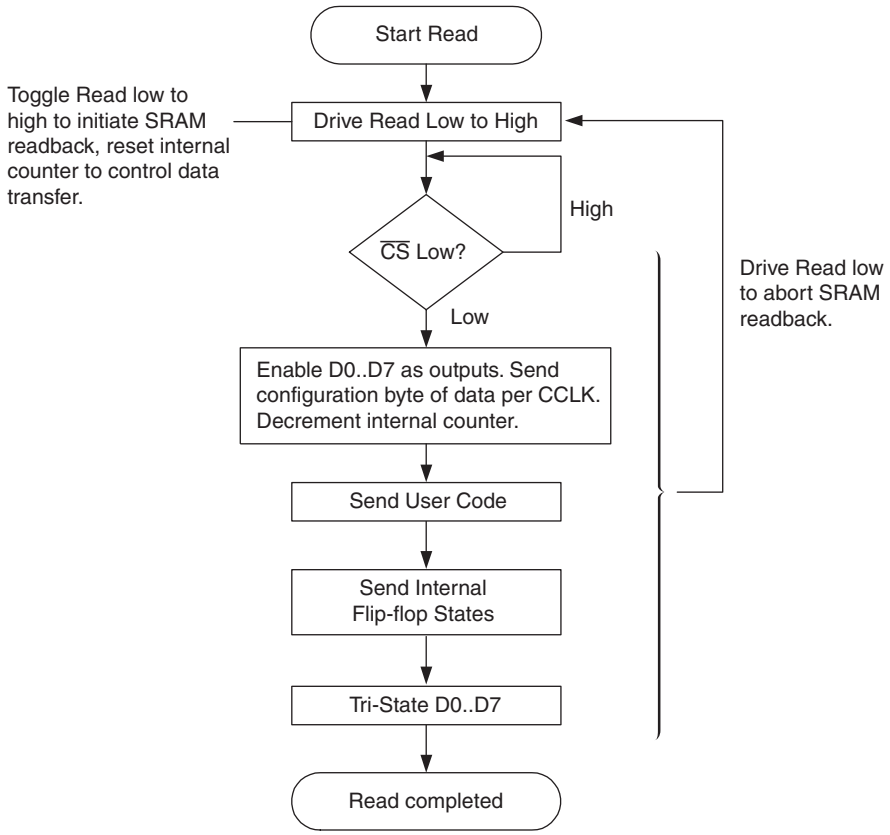
During the read operation, the device will remain functional. On the rising edge of the READ signal, the device will initialize the read state machine, which controls the flow of the data read out from the device. During the read cycle the READ pin must remain high. The $\overline{CS}$ signal is used by the host to control when it is ready to accept data from the ispXPGA device. When the $\overline{CS}$ pin is driven low, data will be read out one byte at a time on the next rising edge of the CCLK pin. A read function is completed when the READ signal goes low or the internal registers have been read out from the device. Figure 23 shows the synchronous peripheral read timing sequence. The flow chart for reading the SRAM is shown in Figure 24.

Figure 23. SRAM Read Cycle Timing



Note: Total SRAM Write Cycle does not occur in five clock cycles.

Figure 24. SRAM Read Cycle Flowchart



Wake-up

Wake-up is a process that is performed when the SRAM has been configured and both the DONE bit is set and CRC has been verified. Wake-Up ensures that the device wakes up gracefully.

If the device has an internal PLL, Wake-Up can also be delayed until selected PLL circuits are “locked”. This feature can be used with any and all combinations of PLLs. For example, the Wake-Up process can be delayed until PLL0 and PLL1 are “locked” or PLL5 and PLL7 are “locked”.

If the user chooses an external signal for PLL feedback rather than an internal clock signal, wake-up must occur without waiting for PLL lock because all I/Os are tri-stated until the device wakes up, preventing the PLL from locking.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPGA devices have boundary scan cells and are compliant with the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board level testing.

Security Scheme

A programmable security scheme is provided on the ispXPGA devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the security scheme prevents read-back of the programmed pattern by a device programmer, securing proprietary designs from competitors. The entire device must be erased in order to erase the security scheme.

Density Shifting

The ispXPGA family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Absolute Maximum Ratings[1, 2, 3]

	1.8V	2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4]	-0.5 to 4.5V	-0.5 to 4.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management technical note is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) + 2) volts is permitted for a duration of <20ns

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V device	1.65	1.95	V
	Supply Voltage for 2.5V device	2.3	2.7	V
	Supply Voltage for 3.3V device	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block for 1.8V device	1.65	1.95	V
	Supply Voltage for PLL block for 2.5V device	2.3	2.7	V
	Supply Voltage for PLL block for 3.3V device	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 1.8V	1.65	1.95	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 2.5V	2.3	2.7	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 3.3V	3.0	3.6	V
T_J (COM)	Junction Temperature Commercial Operation	0	85	C
T_J (IND)	Junction Temperature Industrial Operation	-40	105	C

E²CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}[4]	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-150	µA
		V_{IH} (MAX) $\le V_{IN} \le$ 3.6V	—	—	+/-150	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO}.
2. LVTTL, LVCMOS only
3. $0 < V_{CC} \le V_{CC}$ (MAX), $0 < V_{CCO} \le V_{CCO}$ (MAX)
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-10.0	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	30	—	150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points		V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25°C, f = 1.0MHz.
3. Applies to LVDS buffer.

Supply Current

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}[1, 2]	Standby Core Operating Power Supply Current	V_{CC} = 3.3V	—	TBD	—	mA
		V_{CC} = 2.5V	—	TBD	—	mA
		V_{CC} = 1.8V	—	TBD	—	mA
I_{CCO}[3]	Standby Output Power Supply Current	V_{CCO} = 3.3V	—	TBD	—	mA
		V_{CCO} = 2.5V	—	TBD	—	mA
		V_{CCO} = 1.8V	—	TBD	—	mA
		V_{CCO} = 1.5V	—	TBD	—	mA
I_{CCP}[4]	Standby PLL Operating Supply Current	V_{CCP} = 3.3V	—	TBD	—	mA
		V_{CCP} = 2.5V	—	TBD	—	mA
		V_{CCP} = 1.8V	—	TBD	—	mA
I_{CCJ}[5]	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	100	—	µA
		V_{CCJ} = 2.5V	—	100	—	µA
		V_{CCJ} = 1.8V	—	100	—	µA

1. T_A = 25˚C, frequency = 1.0 MHz, device configured with 16-bit counters.
2. I_{CC} varies with specific device configuration and operating frequency. For more accurate power calculation use the ispXPGA Power Estimator.
3. T_A = 25˚C, per bank, no DC load, frequency = 0 MHz.
4. T_A = 25˚C, per PLL, frequency = 5.0 MHz.
5. T_A = 25˚C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[1]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
PCI-X	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
HSTL Class IV	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS[3]	2.3	2.5	3.6	-	-	-
LVPECL[3]	3.0	3.3	3.6	-	-	-
BLVDS[3]	2.3	2.5	3.6	-	-	-

1. Design tool default setting.
2. Inputs independent of V_{CCO}.
3. For best performance when using LVDS with sysHSI blocks, $2.3V \leq V_{CCO} \leq 2.7V$.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCO} - 0.4	20, 16, 12, 8, 5.33, 4	-20, -16,-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1]	-0.3	0.68[3]	1.07[3]	3.6	0.4	V_{CCO} - 0.4	12, 8[1], 5.33, 4	-12, -8[1], -5.33, -4
		$0.35V_{CC}$	$0.65V_{CC}$		0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCO} - 0.4	20, 16, 12, 8, 5.33, 4	-20, -16,-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3	-0.3	1.08[3]	1.5[3]	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		$0.3V_{CCO}$	0.5 V_{CCO}					
PCI-X	-0.3	Note 3	Note 3	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.35 V_{CCO}	0.5 V_{CCO}					
AGP-1X	-0.3	1.08[3]	1.5[3]	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3 V_{CCO}	0.5 V_{CCO}					
SSTL 3 Class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL 3 Class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL 2 Class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL 2 Class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL Class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL Class IV	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	N/A	36	N/A

1. Design tool default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank
3. Applicable for ispXPGA V/B devices.

sysIO Differential Standards DC Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[1]					
$V_{INP,}$ V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold		+/-100mV	—	—
V_{CM}	Input Common Mode voltage	Half the sum of the two inputs	0.05V	—	2.35V
I_{IN}	Input current	Power on or Power off	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
$V_{INP,}$ V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold		+/-100mV	—	—
V_{CM}	Input Common Mode voltage	Half the sum of the two inputs	0.05V	—	2.35V
I_{IN}	Input current	Power on or Power off	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

ispXPGA External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—		—		—		ns
t_S	Global Clock Input Setup	PIO Input Register without input delay		—		—		—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay		—		—		—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay		—		—		—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay		—		—		—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—		—		—		ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay		—		—		—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay		—		—		—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay		—		—		—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay		—		—		—	ns

ispXPGA PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.39	—	0.44	—	0.55	ns
t_{LUT5}	5-Input LUT Delay	—	0.70	—	0.79	—	0.99	ns
t_{LUT6}	6-Input LUT Delay	—	0.82	—	0.93	—	1.17	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.74	—	-0.70	—	-0.56	—	ns
t_{LSR_H}	Shift Register Hold Time	0.67	—	0.71	—	0.89	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.39	—	0.44	—	0.55	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macrocell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.12	ns
$t_{LCTHRUL}$	MC (Macrocell) Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.07	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.40	—	0.45	—	0.57	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.28	—	0.31	—	0.39	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.34	—	0.39	—	0.49	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.25	—	0.28	—	0.35	ns
Feed-thru								
t_{LFT}	GLB Feed-thru Delay	—	0.14	—	0.16	—	0.20	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.17	—	1.33	—	1.67	ns
t_{LRAMAD_S}	Address Setup Time	-0.42	—	-0.40	—	-0.30	—	ns
t_{LRAMD_S}	Data Setup Time	0.20	—	0.22	—	0.28	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.44	—	0.46	—	0.58	—	ns
t_{LRAMAD_H}	Address Hold Time	0.57	—	0.60	—	0.75	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.14	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.15	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.64	—	3.00	—	3.75	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.82	—	0.93	—	1.17	ns
Register/Latch Delays								
Register								
t_{L_CO}	Register Clock to Output Delay	—	0.55	—	0.62	—	0.78	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.18	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.13	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.14	—	ns
Latch								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.13	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.18	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.13	ns

ispXPGA PFU Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.03	—	1.17	—	1.47	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	—	2.64	—	3.00	—	3.75	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.49	—	0.55	—	0.69	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

Timing v.1.1

ispXPGA PIC Timing Parameters

Parameter	Description		-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays									
t_{IO_CO}	Register Clock to Output Delay		—	0.96	—	1.09	—	1.37	ns
t_{IO_S}	Register Setup Time (Data Before Clock)		0.05	—	0.05	—	0.07	—	ns
t_{IO_H}	Register Hold Time (Data After Clock)		0.06	—	0.06	—	0.08	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time		-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time		0.13	—	0.13	—	0.17	—	ns
t_{IO_GO}	Latch Gate to Output Delay		—	0.81	—	0.91	—	1.14	ns
t_{IOL_S}	Latch Setup Time		0.05	—	0.05	—	0.07	—	ns
t_{IOL_H}	Latch Hold Time		0.06	—	0.06	—	0.08	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)		—	0.09	—	0.10	—	0.13	ns
t_{IOASRO}	Asynchronous Set/Reset to Output		—	1.11	—	1.26	—	1.58	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width		—	2.64	—	3.00	—	3.75	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time		—	0.22	—	0.25	—	0.32	ns
Input/Output Delays									
t_{IOBUF}	Output Buffer Delay		—	0.93	—	1.06	—	1.33	ns
t_{IOIN}	Input Buffer Delay		—	0.67	—	0.76	—	0.95	ns
t_{IOOEN}	Output Enable Delay		—	0.50	—	0.56	—	0.70	ns
t_{IOODIS}	Output Disable Delay		—	-0.11	—	-0.10	—	-0.08	ns
Feed-thru									
t_{IOFT}	Feed-thru Delay		—	0.18	—	0.20	—	0.25	ns
Optional Adders		**Base Parameters**							
$t_{IOINDLY}$	Input Delay Adder	—	—	7.02	—	7.98	—	9.98	ns
t_{IOIA}	Input Adjuster Delay	t_{IOBUF}, t_{IOEN}, t_{IODIS}	See sysIO Table						—
t_{IOOA}	Output Adjuster Delay	t_{IOBUF}, t_{IOEN}, t_{IODIS}	See sysIO Table						—

Timing v.1.1

ispXPGA EBR Timing Parameters

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.10	—	0.10	—	0.10	—	ns
t_{EBSWAD_H}	Address Hold Delay	0.22	—	0.23	—	0.29	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.00	—	3.40	—	4.25	—	ns
t_{EBSWCE_S}	Clock Enable Setup Time	0.47	—	0.50	—	0.63	—	ns
t_{EBSWCE_H}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	1.11	—	1.18	—	1.48	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	-1.05	—	-0.99	—	-0.79	—	ns
t_{EBSWD_S}	Data Setup Time	0.00	—	0.00	—	0.10	—	ns
t_{EBSWD_H}	Data Hold Time	0.51	—	0.54	—	0.68	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	0.75	—	0.85	—	1.07	ns
t_{EBSRAD_S}	Address Setup Delay	1.53	—	1.62	—	1.95	—	ns
t_{EBSRAD_H}	Address Hold Delay	-1.27	—	-1.20	—	-0.90	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.00	—	3.40	—	4.25	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	0.47	—	0.50	—	0.63	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	0.43	—	0.45	—	0.56	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	0.61	—	0.69	—	0.87	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.53	—	0.60	—	0.75	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	0.65	—	0.74	—	0.93	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.55	—	0.62	—	0.78	ns
Asynchronous Read								
$t_{EBARADO}$	Address to Valid+Invalid Data Delay	2.13	—	2.41	—	3.02	—	ns
t_{EBARAD_H}	Address to Valid Data Delay	2.13	—	2.41	—	3.02	—	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	0.59	—	0.66	—	0.83	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.51	—	0.58	—	0.73	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	0.68	—	0.77	—	0.97	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.57	—	0.64	—	0.80	ns

Timing v.1.1

ispXPGA Family Timing Adders

Parameter	Description	Base Parameter	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
PCI_X_in	Using PCI-X	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5v, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5v, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3v, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3v, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.6	—	0.6	—	0.6	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA Family Timing Adders (Continued)

Parameter	Description	Base Parameter	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_IV_out	Using HSTL 2.5V, Class IV	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
PCI_X_out	Using PCI-X Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	0.5	—	ns
t_{PWL}	Input clock, low time	20% to 20%	0.5	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 300	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 250	ps
		Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz and 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 100	ps
$T_{JIT(PERIOD)}$	Output clock, period jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 300	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz	—	+/- 150	ps
t_{PHASE}	Input clock to external feedback delta	External feedback	—	500	ps
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 170	+/- 480	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 1.19	+/- 3.36	ns
t_{PLL_RSTR}	Reset recovery time of the M-divider		—	—	ns
t_{PLL_RSTW}	Minimum reset pulse width		—	1.5	ns

Timing v.1.1

1. This condition assures that the output phase jitter will remain within specification
2. Accumulated jitter measured over 10,000 waveform samples

sysHSI Internal Timing

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
sysHSI Block Delays								
$t_{HSIOUTVALIDPOST}$	RDX, LOSS, CDRLOCK, SYDT Valid After RECCLK Falling Edge							ns
$t_{HSIOUTVALIDPRE}$	RDX, LOSS, CDRLOCK, SYDT Valid Before RECCLK Falling Edge							ns
$t_{HSITDXDATAH}$	TDX Data Hold Time							ns
$t_{HSITDXDATAS}$	TDX Data Setup Time							ns

Timing v.1.1

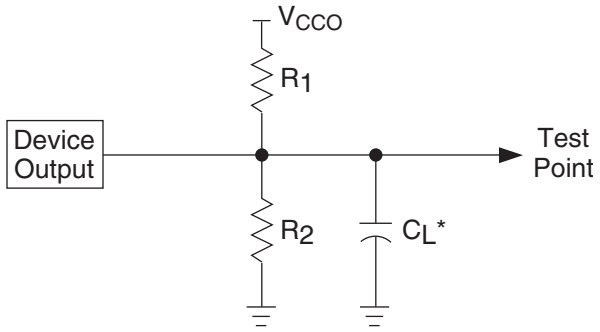
Boundary Scan Timing

Parameter	Description	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	16	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	16	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	16	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	20	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	20	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	20	ns

Switching Test Conditions

Figure 25 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 10.

Figure 25. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes test fixture and probe capacitance.

Table 10. Text Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Reference	VCCO
LVCMOS I/O, (L -> H, H -> L)	106	106	35pF	LVCMOS 3.3 = V_{CCO}/2	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	∞	106	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	∞	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	∞	106	5pF	V_{OH} - 0.3	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	∞	5pF	V_{OH} + 0.3	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions[1]

Signal Name	Signal Type	Description
General Purpose		
BK*y*_IO*x*[1,2]	Input/Output	General purpose I/O number x in I/O Bank y
GCLK*n*/I*n*[7]	Input	Global clock/input
GSR	Input	Global Set/Reset
NC	—	No Connect
GND	GND	Ground
V_{CC}	VCC	Core logic power supply
V_{CCJ}	VCC	IEEE 1149.1 TAP power supply
V_{CCOy}[2]	VCC	I/O Bank y power supply
V_{REFy}[2]	Input	I/O Bank y reference voltage
D_{XN}, D_{XP}	Output	Temperature Sensing Diodes, provide a differential voltage, which corresponds to the temperature of the device.
Test and Program/Configuration		
TMS	Input	Test Mode Select
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TOE	Input	Test Output Enable tri-states all I/O pins
CFG0	Input	Selects the SRAM memory configuration type (Peripheral or E^2CMOS Refresh)
$\overline{PROGRAM}$	Input	Initiates download from E^2CMOS or the peripheral port to SRAM memory
DONE	Bi-directional	Indicates when configuration is complete
$\overline{INIT}$	Bi-directional	Indicates the device is ready for programming
READ	Input	Selects the READ operation when in sysCONFIG mode
CCLK	Input	sysCONFIG Configuration Clock
$\overline{CS}$	Input	sysCONFIG Chip Select
D[7:0]	Bi-directional	sysCONFIG Peripheral Port Data I/O
sysCLOCK PLL[3]		
PLL_FBK*z*	Input	Optional external feedback
PLL_RST*z*	Input	Optional external M divider reset
CLK_OUT*z*	Internal Signal	Clock output (routable to any I/O)
PLL_LOCK*z*	Internal Signal	Lock output (routable to any I/O)
GND_P	GND	PLL Ground
V_{CCP}	VCC	PLL power supply
sysHSI Block[4, 5]		
HSI*m*A_SINP, HSI*m*B_SINP	Input	P-side of differential serial data input
HSI*m*A_SINN, HSI*m*B_SINN	Input	N-side of differential serial data input
HSI*m*A_SOUTP, HSI*m*B_SOUTP	Output	P-side of differential serial data output
HSI*m*A_SOUTN, HSI*m*B_SOUTN	Output	N-side of differential serial data output
HSI*m*A_LOSS, HSI*m*B_LOSS	Internal Signal	Detects loss of signal
HSI*m*A_SYDT, HSI*m*B_SYDT	Internal Signal	Symbol alignment detect
HSI*m*A_RECCLK, HSI*m*B_RECCLK	Internal Signal	Recovered clock
HSI*m*A_CDRLOCK, HSI*m*B_CDRLOCK	Internal Signal	Indicates when the CDR circuit is locked

Signal Descriptions[1] (Continued)

Signal Name	Signal Type	Description
HSI*m*A_CDRRST, HSI*m*B_CDRRST	Input	CDR Reset
HSI*m*A_EXLOSS, HSI*m*B_EXLOSS	Input	External loss indicates data on SIN is invalid, forces LOSS to “1”
HSI*m*A_SYDTRST, HSI*m*B_SYDTRST	Input	Synchronous Pattern Detect Reset forces the CDR circuit through the lock-in process
HSI*m*_CSLOCK, HSI*m*_CSLOCK	Internal Signal	Indicates when the CSPLL circuit is locked
sysHSI Block (Source Synchronous Mode)[6]		
SS_CLKIN0P, SS_CLKIN1P	Input	P-side of differential clock input
SSCLKIN0N, SS_CLKIN1N	Input	N-side of differential clock input
SS_CLKOUT0P, SS_CLKOUT1P	Output	P-side of differential clock output
SS_CLKOUT0N, SS_CLKOUT1N	Output	N-side of differential clock output
CAL0, CAL1	Input	Initiates source synchronous calibration sequence

1. x is a variable for the I/O number.
2. y is a variable for the I/O Bank.
3. z is a variable for the PLL number.
4. m is a variable for the sysHSI block number.
5. A and B refer to the sysHSI block channels.
6. 0 and 1 refer to Source Synchronous group 0 and 1
7. n is a variable for the GCLK and Input number

ispXPGA Power Supply and NC Connections[1]

Signals	680-Ball fpBGA	900-Ball fpBGA
VCC	AE35, AE5, AL5, AR15, AR25, AR31, AR35, AR5, AT36, AT4, AU3, AU37, C3, C37, D36, D4, E15, E25, E35, E5, E9, J35, R35, R5	L11, L20, M12, M13, M14, M17, M18, M19, N12, N19, P12, P19, U12, U19, V12, V19, W12, W13, W14, W17, W18, W19, Y11, Y20
VCCO0	E11, E12, E13, E17, E18, E7	K3, L10, M11, N11, N5, P11, R11, R12
VCCO1	E22, E23, E27, E29, E31, E33	AA3, T11, T12, U11, V11, V5, W11, Y10
VCCO2	G35, L35, M35, N35, U35, V35	AA11, AF13, AH10, W15, Y12, Y13, Y14, Y15
VCCO3	AB35, AC35, AG35, AJ35, AL35, AN35	AA20, AF18, AH21, W16, Y16, Y17, Y18, Y19
VCCO4	AR22, AR23, AR27, AR28, AR29, AR33	AA28, T19, T20, U20, V20, V26, W20, Y21
VCCO5	AR11, AR13, AR17, AR18, AR7, AR9	K28, L21, M20, N20, N26, P20, R19, R20
VCCO6	AB5, AC5, AG5, AH5, AJ5, AN5	C21, E18, K20, L16, L17, L18, L19, M16
VCCO7	G5, J5, L5, N5, U5, V5	C10, E13, K11, L12, L13, L14, L15, M15
VCCP	E20, AW22	R5, T26
VCCJ	D3	B3
GND	A1, A2, A20, A38, A39, AE3, AE37, AK3, AK37, AR36, AR4, AT20, AT35, AT5, AU10, AU14, AU20, AU26, AU30, AV1, AV2, AV20, AV38, AV39, AW1, AW2, AW20, AW38, AW39, B1, B2, B20, B38, B39, C10, C14, C20, C26, C30, D20, D35, D5, E36, E4, K3, K37, P37, R3, Y1, Y2, Y3, Y36, Y37, Y38, Y39, Y4	A1, A2, A29, A30, AB28, AB3, AG27, AG4, AH22, AH28, AH3, AH9, AJ1, AJ2, AJ29, AJ30, AK1, AK2, AK29, AK30, B1, B2, B29, B30, C22, C28, C3, C9, D27, D4, J28, J3, N13, N14, N15, N16, N17, N18, P13, P14, P15, P16, P17, P18, R13, R14, R15, R16, R17, R18, T13, T14, T15, T16, T17, T18, U13, U14, U15, U16, U17, U18, V13, V14, V15, V16, V17, V18
GNDP	AR20, A21	R28, T3
NC[2]	A3, B29, AW3, AV3, AW11, AV11, AV29, AW29, AW37, B3, AV37, C39, C38, AU39, AU38, AJ39, AJ38, N38, N39, C2, C1, AU1, AU2, AJ2, AJ1, N2, N1, B11, A11, A37, B37, A29	AA22, AA23, AA24, AA25, AB23, AC24, T21, T22, T23, T24, T25, U21, U22, U23, U24, V21, V22, V23, W21, W22, W23, W24, Y22, Y23, Y24, AA16, AA17, AA18, AA19, AA21, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD16, AD17, AD19, AD20, AD22, AD23, AD24, AE22, AE25, AF25, AF26, AA10, AA12, AA13, AA14, AA15, AB10, AB11, AB12, AB13, AB14, AB15, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC8, AC9, AD11, AD12, AD14, AD15, AD7, AD8, AD9, AE6, AE9, AF5, AF6, H24, J23, K22, K23, K24, K25, L22, L23, L24, M21, M22, M23, M24, N21, N22, N23, P21, P22, P23, P24, R21, R22, R23, R24, R25, AA6, AA7, AA8, AA9, AB8, AC7, T10, T6, T7, T8, T9, U10, U7, U8, U9, V10, V8, V9, W10, W7, W8, W9, Y7, Y8, Y9, H5, H6, H7, J8, K6, K7, K8, K9, L7, L8, L9, M10, M7, M8, M9, N10, N8, N9, P10, P7, P8, P9, R10, R8, R9, E25, E26, F22, F25, G16, G17, G19, G20, G22, G23, G24, H16, H17, H18, H19, H20, H21, H22, H23, J16, J17, J18, J19, J20, J21, J22, K16, K17, K18, K19, K21, E5, E6, F6, F9, G11, G12, G14, G15, G7, G8, G9, H10, H11, H12, H13, H14, H15, H8, H9, J10, J11, J12, J13, J14, J15, J9, K10, K12, K13, K14, K15

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.

ispXPGA Logic Signal Connections: 680-Ball fpBGA

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCCO0	VCCO0		
C4	BK0_IO0		0
B4	BK0_IO1		0
E6	BK0_IO2		1
GND	GND		
D6	BK0_IO3		1
A4	BK0_IO4		2
E8	BK0_IO5		2
C5	BK0_IO6	HSI0A_SOUTP	5
VCCO0	VCCO0		
C6	BK0_IO7	HSI0A_SOUTN	5
A6	BK0_IO8		6
A5	BK0_IO9		6
B6	BK0_IO10	HSI0A_SINP	7
GND	GND		
B5	BK0_IO11	HSI0A_SINN	7
B7	BK0_IO12	VREF0	8
A7	BK0_IO13		8
D8	BK0_IO14	HSI0B_SOUTP	9
VCCO0	VCCO0		
D7	BK0_IO15	HSI0B_SOUTN	9
D9	BK0_IO16		10
E10	BK0_IO17		10
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
C8	BK0_IO18	HSI0B_SINP	11
GND	GND		
C7	BK0_IO19	HSI0B_SINN	11
A8	BK0_IO20		12
A9	BK0_IO21		12
C9	BK0_IO22	HSI1A_SOUTP	13
VCCO0	VCCO0		
B8	BK0_IO23	HSI1A_SOUTN	13
B9	BK0_IO24		14
B10	BK0_IO25		14
D11	BK0_IO26	HSI1A_SINP	15
GND	GND		
D10	BK0_IO27	HSI1A_SINN	15
A10	BK0_IO28		16
C12	BK0_IO29		16
D12	BK0_IO30	HSI1B_SOUTP	17
VCCO0	VCCO0		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
C11	BK0_IO31	HSI1B_SOUTN	17
A12	BK0_IO32		18
A13	BK0_IO33		18
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
B13	BK0_IO34	HSI1B_SINP	19
GND	GND		
B12	BK0_IO35	HSI1B_SINN	19
E14	BK0_IO36		20
D14	BK0_IO37		20
C13	BK0_IO38	HSI2A_SOUTP	37
VCCO0	VCCO0		
D13	BK0_IO39	HSI2A_SOUTN	37
B14	BK0_IO40		38
A14	BK0_IO41		38
C15	BK0_IO42	HSI2A_SINP	39
GND	GND		
D15	BK0_IO43	HSI2A_SINN	39
A15	BK0_IO44		40
C16	BK0_IO45		40
B15	BK0_IO46	HSI2B_SOUTP	41
VCCO0	VCCO0		
B16	BK0_IO47	HSI2B_SOUTN	41
A16	BK0_IO48		42
B17	BK0_IO49		42
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
D16	BK0_IO50	HSI2B_SINP	43
GND	GND		
E16	BK0_IO51	HSI2B_SINN	43
D17	BK0_IO52		44
C17	BK0_IO53		44
A18	BK0_IO54	PLL_RST0	53
VCCO0	VCCO0		
D18	BK0_IO55	PLL_RST1	53
A17	BK0_IO56		54
E19	BK0_IO57		54
A19	BK0_IO58	PLL_FBK0	55
GND	GND		
B19	BK0_IO59	PLL_FBK1	55

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
C18	BK0_IO60	CLK_OUT0	56
VCCO0	VCCO0		
B18	BK0_IO61	CLK_OUT1	56
GND	GND		
D19	GCLK0		
C19	GCLK1		
E20	VCCP0		
A21	GNDP0		
B21	GCLK2		
C21	GCLK3		
GND	GND		
B23	BK1_IO0	CLK_OUT2	57
VCCO1	VCCO1		
C23	BK1_IO1	CLK_OUT3	57
B22	BK1_IO2	SS_CLKOUT0P	58
GND	GND		
C22	BK1_IO3	SS_CLKOUT0N	58
D21	BK1_IO4	PLL_FBK2	59
E21	BK1_IO5	PLL_FBK3	59
B24	BK1_IO6	SS_CLKIN0P	60
VCCO1	VCCO1		
C24	BK1_IO7	SS_CLKIN0N	60
A22	BK1_IO8		69
D22	BK1_IO9		69
A23	BK1_IO10		70
GND	GND		
B25	BK1_IO11		70
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
D23	BK1_IO12	PLL_RST2	71
A24	BK1_IO13	PLL_RST3	71
A25	BK1_IO14		72
VCCO1	VCCO1		
E24	BK1_IO15		72
D24	BK1_IO16		73
A26	BK1_IO17		73
D25	BK1_IO18		74
GND	GND		
C25	BK1_IO19		74
B26	BK1_IO20		75
B27	BK1_IO21		75
D26	BK1_IO22		76

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCCO1	VCCO1		
A27	BK1_IO23		76
A28	BK1_IO24		93
E26	BK1_IO25		93
C27	BK1_IO26	HSI3A_SOUTP	94
GND	GND		
D27	BK1_IO27	HSI3A_SOUTN	94
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
B28	BK1_IO28		95
A30	BK1_IO29		95
C28	BK1_IO30	HSI3A_SINP	96
VCCO1	VCCO1		
D28	BK1_IO31	HSI3A_SINN	96
A31	BK1_IO32		97
B30	BK1_IO33		97
E28	BK1_IO34	HSI3B_SOUTP	98
GND	GND		
D29	BK1_IO35	HSI3B_SOUTN	98
C29	BK1_IO36		99
B31	BK1_IO37		99
D30	BK1_IO38	HSI3B_SINP	100
VCCO1	VCCO1		
E30	BK1_IO39	HSI3B_SINN	100
A32	BK1_IO40		101
C31	BK1_IO41		101
D31	BK1_IO42	HSI4A_SOUTP	102
GND	GND		
C32	BK1_IO43	HSI4A_SOUTN	102
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
B32	BK1_IO44		103
A33	BK1_IO45		103
C33	BK1_IO46	HSI4A_SINP	104
VCCO1	VCCO1		
B33	BK1_IO47	HSI4A_SINN	104
A34	BK1_IO48		105
A35	BK1_IO49	VREF1	105
D32	BK1_IO50	HSI4B_SOUTP	106
GND	GND		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
D33	BK1_IO51	HSI4B_SOUTN	106
E32	BK1_IO52		107
C34	BK1_IO53		107
B34	BK1_IO54	HSI4B_SINP	108
VCCO1	VCCO1		
B35	BK1_IO55	HSI4B_SINN	108
A36	BK1_IO56		111
D34	BK1_IO57		111
C35	BK1_IO58		112
GND	GND		
E34	BK1_IO59		112
B36	BK1_IO60		113
C36	BK1_IO61		113
VCCO1	VCCO1		
D39	TCK		
D37	TMS		
D38	TOE		
VCCO2	VCCO2		
E37	BK2_IO0		116
F35	BK2_IO1		116
E39	BK2_IO2		117
GND	GND		
F39	BK2_IO3		117
F36	BK2_IO4		118
E38	BK2_IO5		118
G38	BK2_IO6		121
VCCO2	VCCO2		
F37	BK2_IO7		121
G36	BK2_IO8		122
G39	BK2_IO9		122
H35	BK2_IO10		123
GND	GND		
F38	BK2_IO11		123
J37	BK2_IO12	VREF2	128
H36	BK2_IO13		128
G37	BK2_IO14		129
VCCO2	VCCO2		
H37	BK2_IO15		129
H39	BK2_IO16		134
K35	BK2_IO17		134
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
J36	BK2_IO18		135
GND	GND		
K36	BK2_IO19		135
H38	BK2_IO20		136
J38	BK2_IO21		136
J39	BK2_IO22		137
VCCO2	VCCO2		
L36	BK2_IO23		137
K38	BK2_IO24		140
M36	BK2_IO25		140
L37	BK2_IO26		141
GND	GND		
K39	BK2_IO27		141
L38	BK2_IO28		143
P35	BK2_IO29		143
N36	BK2_IO30		144
VCCO2	VCCO2		
M37	BK2_IO31		144
L39	BK2_IO32		145
M38	BK2_IO33		145
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
M39	BK2_IO34		148
GND	GND		
P36	BK2_IO35		148
R36	BK2_IO36		149
N37	BK2_IO37		149
P38	BK2_IO38		150
VCCO2	VCCO2		
T35	BK2_IO39		150
R37	BK2_IO40		151
R38	BK2_IO41		151
P39	BK2_IO42		152
GND	GND		
R39	BK2_IO43		152
T38	BK2_IO44		153
T36	BK2_IO45		153
T37	BK2_IO46		160
VCCO2	VCCO2		
U36	BK2_IO47		160
U37	BK2_IO48		161
T39	BK2_IO49		161

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
V36	BK2_IO50		162
GND	GND		
U38	BK2_IO51		162
U39	BK2_IO52		163
V38	BK2_IO53		163
V37	BK2_IO54		166
VCCO2	VCCO2		
W36	BK2_IO55		166
W35	BK2_IO56		167
V39	BK2_IO57		167
W37	BK2_IO58		168
GND	GND		
W38	BK2_IO59		168
W39	BK2_IO60		169
VCCO2	VCCO2		
AA39	BK2_IO61		169
GND	GND		
GND	GND		
AA38	BK3_IO0		172
VCCO3	VCCO3		
Y35	BK3_IO1		172
AA37	BK3_IO2		173
GND	GND		
AA35	BK3_IO3		173
AB39	BK3_IO4		174
AB38	BK3_IO5		174
AA36	BK3_IO6		175
VCCO3	VCCO3		
AB37	BK3_IO7		175
AC39	BK3_IO8		178
AC38	BK3_IO9		178
AB36	BK3_IO10		179
GND	GND		
AC37	BK3_IO11		179
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AC36	BK3_IO12		180
AD39	BK3_IO13		180

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AD37	BK3_IO14		182
VCCO3	VCCO3		
AD36	BK3_IO15		182
AD35	BK3_IO16		187
AE38	BK3_IO17		187
AD38	BK3_IO18		188
GND	GND		
AE39	BK3_IO19		188
AF38	BK3_IO20		189
AF37	BK3_IO21		189
AF39	BK3_IO22		190
VCCO3	VCCO3		
AE36	BK3_IO23		190
AF36	BK3_IO24		191
AG38	BK3_IO25		191
AG39	BK3_IO26		193
GND	GND		
AG37	BK3_IO27		193
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AH37	BK3_IO28		197
AH38	BK3_IO29		197
AG36	BK3_IO30		198
VCCO3	VCCO3		
AH39	BK3_IO31		198
AK39	BK3_IO32		200
AK38	BK3_IO33		200
AF35	BK3_IO34		201
GND	GND		
AJ37	BK3_IO35		201
AH36	BK3_IO36		202
AM39	BK3_IO37		202
AL38	BK3_IO38		205
VCCO3	VCCO3		
AL39	BK3_IO39		205
AJ36	BK3_IO40		206
AH35	BK3_IO41		206
AL37	BK3_IO42		207
GND	GND		
AN38	BK3_IO43		207
GND	GND		
VCC	VCC		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
GND	GND		
VCC	VCC		
AM38	BK3_IO44		209
AK36	BK3_IO45		209
AM37	BK3_IO46		212
VCCO3	VCCO3		
AN37	BK3_IO47		212
AN39	BK3_IO48		213
AL36	BK3_IO49	VREF3	213
AK35	BK3_IO50		220
GND	GND		
AP39	BK3_IO51		220
AM36	BK3_IO52		221
AP38	BK3_IO53		221
AR39	BK3_IO54		222
VCCO3	VCCO3		
AN36	BK3_IO55		222
AM35	BK3_IO56		225
AR38	BK3_IO57		225
AP37	BK3_IO58		226
GND	GND		
AT39	BK3_IO59		226
AR37	BK3_IO60		227
AP36	BK3_IO61		227
VCCO3	VCCO3		
AT38	RESET		
AP35	DXP		
AT37	DXN		
VCCO4	VCCO4		
AU36	BK4_IO0		228
AV36	BK4_IO1		228
AR34	BK4_IO2		229
GND	GND		
AW36	BK4_IO3		229
AW35	BK4_IO4		230
AV35	BK4_IO5		230
AV34	BK4_IO6	HSI5A_SINN	233
VCCO4	VCCO4		
AU34	BK4_IO7	HSI5A_SINP	233
AT34	BK4_IO8		234
AU35	BK4_IO9		234
AT33	BK4_IO10	HSI5A_SOUTN	235
GND	GND		
AU33	BK4_IO11	HSI5A_SOUTP	235

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AW34	BK4_IO12	VREF4	236
AV33	BK4_IO13		236
AR32	BK4_IO14	HSI5B_SINN	237
VCCO4	VCCO4		
AT32	BK4_IO15	HSI5B_SINP	237
AU32	BK4_IO16		238
AW33	BK4_IO17		238
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AV32	BK4_IO18	HSI5B_SOUTN	239
GND	GND		
AV31	BK4_IO19	HSI5B_SOUTP	239
AU31	BK4_IO20		240
AW32	BK4_IO21		240
AR30	BK4_IO22	HSI6A_SINN	241
VCCO4	VCCO4		
AT31	BK4_IO23	HSI6A_SINP	241
AW31	BK4_IO24		242
AV30	BK4_IO25		242
AT30	BK4_IO26	HSI6A_SOUTN	243
GND	GND		
AT29	BK4_IO27	HSI6A_SOUTP	243
AW30	BK4_IO28		244
AU29	BK4_IO29		244
AT28	BK4_IO30	HSI6B_SINN	245
VCCO4	VCCO4		
AU28	BK4_IO31	HSI6B_SINP	245
AV28	BK4_IO32		246
AT27	BK4_IO33		246
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AU27	BK4_IO34	HSI6B_SOUTN	247
GND	GND		
AV27	BK4_IO35	HSI6B_SOUTP	247
AW28	BK4_IO36		248
AR26	BK4_IO37		248
AW27	BK4_IO38		265
VCCO4	VCCO4		
AT26	BK4_IO39		265
AV26	BK4_IO40		266

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AR24	BK4_IO41		266
AT25	BK4_IO42		267
GND	GND		
AW26	BK4_IO43		267
AV25	BK4_IO44		268
AT24	BK4_IO45		268
AU24	BK4_IO46		269
VCCO4	VCCO4		
AU25	BK4_IO47		269
AW25	BK4_IO48	PLL_RST4	270
AW24	BK4_IO49	PLL_RST5	270
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AU23	BK4_IO50		271
GND	GND		
AT23	BK4_IO51		271
AV24	BK4_IO52		272
AW23	BK4_IO53		272
AV23	BK4_IO54	SS_CLKIN1N	281
VCCO4	VCCO4		
AU22	BK4_IO55	SS_CLKIN1P	281
AR21	BK4_IO56	PLL_FBK4	282
AT22	BK4_IO57	PLL_FBK5	282
AV22	BK4_IO58	SS_CLKOUT1N	283
GND	GND		
AV21	BK4_IO59	SS_CLKOUT1P	283
AT21	BK4_IO60	CLK_OUT4	284
VCCO4	VCCO4		
AU21	BK4_IO61	CLK_OUT5	284
GND	GND		
AT19	GCLK4		
AU19	GCLK5		
AW22	VCCP1		
AR20	GNDP1		
AU18	GCLK6		
AT18	GCLK7		
GND	GND		
AV17	BK5_IO0	CLK_OUT6	285
VCCO5	VCCO5		
AV18	BK5_IO1	CLK_OUT7	285
AW21	BK5_IO2	PLL_FBK6	286
GND	GND		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AV19	BK5_IO3	PLL_FBK7	286
AR19	BK5_IO4		287
AW19	BK5_IO5		287
AW18	BK5_IO6	PLL_RST6	288
VCCO5	VCCO5		
AW17	BK5_IO7	PLL_RST7	288
AT17	BK5_IO8		297
AV16	BK5_IO9		297
AU17	BK5_IO10	HSI7A_SINN	298
GND	GND		
AT16	BK5_IO11	HSI7A_SINP	298
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AW16	BK5_IO12		299
AU16	BK5_IO13		299
AV14	BK5_IO14	HSI7A_SOUTN	300
VCCO5	VCCO5		
AV15	BK5_IO15	HSI7A_SOUTP	300
AU15	BK5_IO16		301
AW15	BK5_IO17		301
AT15	BK5_IO18	HSI7B_SINN	302
GND	GND		
AR16	BK5_IO19	HSI7B_SINP	302
AW14	BK5_IO20		303
AW13	BK5_IO21		303
AR14	BK5_IO22	HSI7B_SOUTN	304
VCCO5	VCCO5		
AT14	BK5_IO23	HSI7B_SOUTP	304
AT13	BK5_IO24		321
AV13	BK5_IO25		321
AU12	BK5_IO26	HSI8A_SINN	322
GND	GND		
AU13	BK5_IO27	HSI8A_SINP	322
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AV12	BK5_IO28		323
AT12	BK5_IO29		323
AR12	BK5_IO30	HSI8A_SOUTN	324
VCCO5	VCCO5		
AT11	BK5_IO31	HSI8A_SOUTP	324

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AW12	BK5_IO32		325
AU11	BK5_IO33		325
AV9	BK5_IO34	HSI8B_SINN	326
GND	GND		
AV10	BK5_IO35	HSI8B_SINP	326
AW10	BK5_IO36		327
AW9	BK5_IO37		327
AT10	BK5_IO38	HSI8B_SOUTN	328
VCCO5	VCCO5		
AU9	BK5_IO39	HSI8B_SOUTP	328
AT9	BK5_IO40		329
AR10	BK5_IO41		329
AU8	BK5_IO42	HSI9A_SINN	330
GND	GND		
AV8	BK5_IO43	HSI9A_SINP	330
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AW8	BK5_IO44		331
AW7	BK5_IO45		331
AU7	BK5_IO46	HSI9A_SOUTN	332
VCCO5	VCCO5		
AT8	BK5_IO47	HSI9A_SOUTP	332
AV7	BK5_IO48		333
AW6	BK5_IO49	VREF5	333
AU6	BK5_IO50	HSI9B_SINN	334
GND	GND		
AV6	BK5_IO51	HSI9B_SINP	334
AR8	BK5_IO52		335
AT7	BK5_IO53		335
AU5	BK5_IO54	HSI9B_SOUTN	336
VCCO5	VCCO5		
AV5	BK5_IO55	HSI9B_SOUTP	336
AW5	BK5_IO56		339
AW4	BK5_IO57		339
AT6	BK5_IO58		340
GND	GND		
AV4	BK5_IO59		340
AR6	BK5_IO60		341
AU4	BK5_IO61		341
VCCO5	VCCO5		
AT1	CFG0		
AT3	DONE		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AT2	PROGRAMB		
VCCO6	VCCO6		
AP4	BK6_IO0	INITB	342
AP5	BK6_IO1	CCLK	342
AR3	BK6_IO2		343
GND	GND		
AR2	BK6_IO3		343
AP3	BK6_IO4	CSB	345
AR1	BK6_IO5	Read	345
AP2	BK6_IO6		349
VCCO6	VCCO6		
AP1	BK6_IO7		349
AN4	BK6_IO8		350
AM5	BK6_IO9		350
AN3	BK6_IO10		351
GND	GND		
AN2	BK6_IO11		351
AM4	BK6_IO12	VREF6	356
AM3	BK6_IO13		356
AN1	BK6_IO14		358
VCCO6	VCCO6		
AM2	BK6_IO15		358
AL4	BK6_IO16		359
AK5	BK6_IO17		359
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AM1	BK6_IO18		362
GND	GND		
AK4	BK6_IO19		362
AL3	BK6_IO20		363
AL2	BK6_IO21		363
AL1	BK6_IO22		364
VCCO6	VCCO6		
AK2	BK6_IO23		364
AK1	BK6_IO24		365
AJ4	BK6_IO25		365
AJ3	BK6_IO26		366
GND	GND		
AH4	BK6_IO27		366
AH3	BK6_IO28		367
AH2	BK6_IO29		367
AH1	BK6_IO30		368

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCCO6	VCCO6		
AG4	BK6_IO31		368
AF5	BK6_IO32	DATA7	371
AG3	BK6_IO33	DATA6	371
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AG2	BK6_IO34		372
GND	GND		
AF4	BK6_IO35		372
AF3	BK6_IO36	DATA5	374
AG1	BK6_IO37	DATA4	374
AE2	BK6_IO38		375
VCCO6	VCCO6		
AF1	BK6_IO39		375
AF2	BK6_IO40		382
AE1	BK6_IO41		382
AE4	BK6_IO42		384
GND	GND		
AD4	BK6_IO43		384
AD5	BK6_IO44		385
AD3	BK6_IO45		385
AD2	BK6_IO46		386
VCCO6	VCCO6		
AD1	BK6_IO47		386
AC4	BK6_IO48		387
AC3	BK6_IO49		387
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AC2	BK6_IO50	DATA3	388
GND	GND		
AC1	BK6_IO51	DATA2	388
AB3	BK6_IO52		389
AB4	BK6_IO53		389
AB2	BK6_IO54	DATA1	394
VCCO6	VCCO6		
AB1	BK6_IO55	DATA0	394
AA3	BK6_IO56		395
AA4	BK6_IO57		395
AA5	BK6_IO58		396
GND	GND		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AA2	BK6_IO59		396
AA1	BK6_IO60		397
VCCO6	VCCO6		
Y5	BK6_IO61		397
GND	GND		
GND	GND		
W3	BK7_IO0		399
VCCO7	VCCO7		
W1	BK7_IO1		399
W2	BK7_IO2		400
GND	GND		
W4	BK7_IO3		400
V1	BK7_IO4		401
V2	BK7_IO5		401
V3	BK7_IO6		403
VCCO7	VCCO7		
V4	BK7_IO7		403
W5	BK7_IO8		409
U1	BK7_IO9		409
U2	BK7_IO10		411
GND	GND		
U3	BK7_IO11		411
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
U4	BK7_IO12		412
T1	BK7_IO13		412
T2	BK7_IO14		413
VCCO7	VCCO7		
T3	BK7_IO15		413
R1	BK7_IO16		415
R2	BK7_IO17		415
T4	BK7_IO18		416
GND	GND		
P1	BK7_IO19		416
P2	BK7_IO20		417
P3	BK7_IO21		417
R4	BK7_IO22		424
VCCO7	VCCO7		
T5	BK7_IO23		424
M1	BK7_IO24		425
M2	BK7_IO25		425
N3	BK7_IO26		426

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
GND	GND		
P4	BK7_IO27		426
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
L1	BK7_IO28		427
M3	BK7_IO29		427
L2	BK7_IO30		428
VCCO7	VCCO7		
N4	BK7_IO31		428
K1	BK7_IO32		429
K2	BK7_IO33		429
P5	BK7_IO34		430
GND	GND		
L3	BK7_IO35		430
J1	BK7_IO36		432
J2	BK7_IO37		432
M4	BK7_IO38		433
VCCO7	VCCO7		
H1	BK7_IO39		433
J3	BK7_IO40		434
L4	BK7_IO41		434
M5	BK7_IO42		435
GND	GND		
H2	BK7_IO43		435
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
K4	BK7_IO44		439
G1	BK7_IO45		439
H3	BK7_IO46		441
VCCO7	VCCO7		
J4	BK7_IO47	VREF7	441
K5	BK7_IO48		446
G3	BK7_IO49		446
H4	BK7_IO50		447
GND	GND		
F2	BK7_IO51		447
G2	BK7_IO52		448
H5	BK7_IO53		448
F3	BK7_IO54		449
VCCO7	VCCO7		

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

680-Ball fpBGA	Signal Name	Second Function	LVDS Pair
F1	BK7_IO55		449
G4	BK7_IO56		453
E1	BK7_IO57		453
F4	BK7_IO58		454
GND	GND		
E2	BK7_IO59		454
F5	BK7_IO60		455
E3	BK7_IO61		455
VCCO7	VCCO7		
D2	TDO		
D3	VCCJ		
D1	TDI		

ispXPGA Logic Signal Connections: 900-Ball fpBGA

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCCO0	VCCO0		
D3	BK0_IO0		0
E3	BK0_IO1		0
C2	BK0_IO2		1
GND	GND (Bank 0)		
C1	BK0_IO3		1
E4	BK0_IO4		2
F5	BK0_IO5		2
D2	BK0_IO6	HSI0A_SOUTP	5
VCCO0	VCCO0		
D1	BK0_IO7	HSI0A_SOUTN	5
F4	BK0_IO8		6
F3	BK0_IO9		6
E2	BK0_IO10	HSI0A_SINP	7
GND	GND (Bank 0)		
E1	BK0_IO11	HSI0A_SINN	7
G6	BK0_IO12	VREF0	8
G5	BK0_IO13		8
F1	BK0_IO14	HSI0B_SOUTP	9
VCCO0	VCCO0		
F2	BK0_IO15	HSI0B_SOUTN	9
G4	BK0_IO16		10
G3	BK0_IO17		10
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
G2	BK0_IO18	HSI0B_SINP	11
GND	GND (Bank 0)		
G1	BK0_IO19	HSI0B_SINN	11
H3	BK0_IO20		12
H4	BK0_IO21		12
H1	BK0_IO22	HSI1A_SOUTP	13
VCCO0	VCCO0		
H2	BK0_IO23	HSI1A_SOUTN	13
J7	BK0_IO24		14
J6	BK0_IO25		14
J1	BK0_IO26	HSI1A_SINP	15
GND	GND (Bank 0)		
J2	BK0_IO27	HSI1A_SINN	15
J4	BK0_IO28		16
J5	BK0_IO29		16
K1	BK0_IO30	HSI1B_SOUTP	17
VCCO0	VCCO0		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
K2	BK0_IO31	HSI1B_SOUTN	17
K5	BK0_IO32		18
K4	BK0_IO33		18
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
L1	BK0_IO34	HSI1B_SINP	19
GND	GND (Bank 0)		
L2	BK0_IO35	HSI1B_SINN	19
L6	BK0_IO36		20
L5	BK0_IO37		20
M1	BK0_IO38	HSI2A_SOUTP	37
VCCO0	VCCO0		
M2	BK0_IO39	HSI2A_SOUTN	37
L3	BK0_IO40		38
L4	BK0_IO41		38
M6	BK0_IO42	HSI2A_SINP	39
GND	GND (Bank 0)		
M5	BK0_IO43	HSI2A_SINN	39
M4	BK0_IO44		40
M3	BK0_IO45		40
N1	BK0_IO46	HSI2B_SOUTP	41
VCCO0	VCCO0		
N2	BK0_IO47	HSI2B_SOUTN	41
N7	BK0_IO48		42
N6	BK0_IO49		42
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
P1	BK0_IO50	HSI2B_SINP	43
GND	GND (Bank 0)		
P2	BK0_IO51	HSI2B_SINN	43
N3	BK0_IO52		44
N4	BK0_IO53		44
P6	BK0_IO54	PLL_RST0	53
VCCO0	VCCO0		
P5	BK0_IO55	PLL_RST1	53
P3	BK0_IO56		54
P4	BK0_IO57		54
R7	BK0_IO58	PLL_FBK0	55
GND	GND (Bank 0)		
R6	BK0_IO59	PLL_FBK1	55

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
R1	BK0_IO60	CLK_OUT0	56
VCCO0	VCCO0		
R2	BK0_IO61	CLK_OUT1	56
GND	GND (Bank 0)		
R3	GCLK0		
R4	GCLK1		
R5	VCCP0		
T3	GNDP0		
T4	GCLK2		
T5	GCLK3		
GND	GND (Bank 1)		
T2	BK1_IO0	CLK_OUT2	57
VCCO1	VCCO1		
T1	BK1_IO1	CLK_OUT3	57
U2	BK1_IO2	SS_CLKOUT0P	58
GND	GND (Bank 1)		
U1	BK1_IO3	SS_CLKOUT0N	58
U3	BK1_IO4	PLL_FBK2	59
U4	BK1_IO5	PLL_FBK3	59
V1	BK1_IO6	SS_CLKIN0P	60
VCCO1	VCCO1		
V2	BK1_IO7	SS_CLKIN0N	60
U5	BK1_IO8		69
U6	BK1_IO9		69
V4	BK1_IO10		70
GND	GND (Bank 1)		
V3	BK1_IO11		70
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
V6	BK1_IO12	PLL_RST2	71
V7	BK1_IO13	PLL_RST3	71
W1	BK1_IO14		72
VCCO1	VCCO1		
W2	BK1_IO15		72
W3	BK1_IO16		73
W4	BK1_IO17		73
W5	BK1_IO18		74
GND	GND (Bank 1)		
W6	BK1_IO19		74
Y6	BK1_IO20		75
Y5	BK1_IO21		75
Y4	BK1_IO22		76

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCCO1	VCCO1		
Y3	BK1_IO23		76
AA5	BK1_IO24		93
AA4	BK1_IO25		93
Y2	BK1_IO26	HSI3A_SOUTP	94
GND	GND (Bank 1)		
Y1	BK1_IO27	HSI3A_SOUTN	94
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AB7	BK1_IO28		95
AB6	BK1_IO29		95
AA2	BK1_IO30	HSI3A_SINP	96
VCCO1	VCCO1		
AA1	BK1_IO31	HSI3A_SINN	96
AB5	BK1_IO32		97
AB4	BK1_IO33		97
AB2	BK1_IO34	HSI3B_SOUTP	98
GND	GND (Bank 1)		
AB1	BK1_IO35	HSI3B_SOUTN	98
AC6	BK1_IO36		99
AC5	BK1_IO37		99
AC2	BK1_IO38	HSI3B_SINP	100
VCCO1	VCCO1		
AC1	BK1_IO39	HSI3B_SINN	100
AC4	BK1_IO40		101
AC3	BK1_IO41		101
AD2	BK1_IO42	HSI4A_SOUTP	102
GND	GND (Bank 1)		
AD1	BK1_IO43	HSI4A_SOUTN	102
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AD3	BK1_IO44		103
AD4	BK1_IO45		103
AE2	BK1_IO46	HSI4A_SINP	104
VCCO1	VCCO1		
AE1	BK1_IO47	HSI4A_SINN	104
AD5	BK1_IO48		105
AD6	BK1_IO49	VREF1	105
AF2	BK1_IO50	HSI4B_SOUTP	106
GND	GND (Bank 1)		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AF1	BK1_IO51	HSI4B_SOUTN	106
AE3	BK1_IO52		107
AE4	BK1_IO53		107
AG1	BK1_IO54	HSI4B_SINP	108
VCCO1	VCCO1		
AG2	BK1_IO55	HSI4B_SINN	108
AE5	BK1_IO56		111
AF4	BK1_IO57		111
AH1	BK1_IO58		112
GND	GND (Bank 1)		
AH2	BK1_IO59		112
AF3	BK1_IO60		113
AG3	BK1_IO61		113
VCCO1	VCCO1		
AH4	TCK		
AJ3	TMS		
AK3	TOE		
VCCO2	VCCO2		
AG5	BK2_IO0		116
AH5	BK2_IO1		116
AJ4	BK2_IO2		117
GND	GND (Bank 2)		
AK4	BK2_IO3		117
AG6	BK2_IO4		118
AH6	BK2_IO5		118
AJ5	BK2_IO6		121
VCCO2	VCCO2		
AK5	BK2_IO7		121
AE7	BK2_IO8		122
AF7	BK2_IO9		122
AG7	BK2_IO10		123
GND	GND (Bank 2)		
AH7	BK2_IO11		123
AE8	BK2_IO12	VREF2	128
AF8	BK2_IO13		128
AJ6	BK2_IO14		129
VCCO2	VCCO2		
AK6	BK2_IO15		129
AG8	BK2_IO16		134
AH8	BK2_IO17		134
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AJ7	BK2_IO18		135
GND	GND (Bank 2)		
AK7	BK2_IO19		135
AF9	BK2_IO20		136
AG9	BK2_IO21		136
AJ8	BK2_IO22		137
VCCO2	VCCO2		
AK8	BK2_IO23		137
AD10	BK2_IO24		140
AE10	BK2_IO25		140
AJ9	BK2_IO26		141
GND	GND (Bank 2)		
AK9	BK2_IO27		141
AF10	BK2_IO28		143
AG10	BK2_IO29		143
AK10	BK2_IO30		144
VCCO2	VCCO2		
AJ10	BK2_IO31		144
AE11	BK2_IO32		145
AF11	BK2_IO33		145
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AG11	BK2_IO34		148
GND	GND (Bank 2)		
AH11	BK2_IO35		148
AE12	BK2_IO36		149
AF12	BK2_IO37		149
AJ11	BK2_IO38		150
VCCO2	VCCO2		
AK11	BK2_IO39		150
AG12	BK2_IO40		151
AH12	BK2_IO41		151
AK12	BK2_IO42		152
GND	GND (Bank 2)		
AJ12	BK2_IO43		152
AD13	BK2_IO44		153
AE13	BK2_IO45		153
AK13	BK2_IO46		160
VCCO2	VCCO2		
AJ13	BK2_IO47		160
AG13	BK2_IO48		161
AH13	BK2_IO49		161

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AE14	BK2_IO50		162
GND	GND (Bank 2)		
AF14	BK2_IO51		162
AG14	BK2_IO52		163
AH14	BK2_IO53		163
AJ14	BK2_IO54		166
VCCO2	VCCO2		
AK14	BK2_IO55		166
AE15	BK2_IO56		167
AF15	BK2_IO57		167
AG15	BK2_IO58		168
GND	GND (Bank 2)		
AH15	BK2_IO59		168
AJ15	BK2_IO60		169
VCCO2	VCCO2		
AK15	BK2_IO61		169
GND	GND (Bank 2)		
GND	GND (Bank 3)		
AK16	BK3_IO0		172
VCCO3	VCCO3		
AJ16	BK3_IO1		172
AH16	BK3_IO2		173
GND	GND (Bank 3)		
AG16	BK3_IO3		173
AF16	BK3_IO4		174
AE16	BK3_IO5		174
AK17	BK3_IO6		175
VCCO3	VCCO3		
AJ17	BK3_IO7		175
AH17	BK3_IO8		178
AG17	BK3_IO9		178
AF17	BK3_IO10		179
GND	GND (Bank 3)		
AE17	BK3_IO11		179
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AH18	BK3_IO12		180
AG18	BK3_IO13		180

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AJ18	BK3_IO14		182
VCCO3	VCCO3		
AK18	BK3_IO15		182
AE18	BK3_IO16		187
AD18	BK3_IO17		187
AJ19	BK3_IO18		188
GND	GND (Bank 3)		
AK19	BK3_IO19		188
AH19	BK3_IO20		189
AG19	BK3_IO21		189
AK20	BK3_IO22		190
VCCO3	VCCO3		
AJ20	BK3_IO23		190
AF19	BK3_IO24		191
AE19	BK3_IO25		191
AH20	BK3_IO26		193
GND	GND (Bank 3)		
AG20	BK3_IO27		193
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
AF20	BK3_IO28		197
AE20	BK3_IO29		197
AJ21	BK3_IO30		198
VCCO3	VCCO3		
AK21	BK3_IO31		198
AG21	BK3_IO32		200
AF21	BK3_IO33		200
AK22	BK3_IO34		201
GND	GND (Bank 3)		
AJ22	BK3_IO35		201
AE21	BK3_IO36		202
AD21	BK3_IO37		202
AG22	BK3_IO38		205
VCCO3	VCCO3		
AF22	BK3_IO39		205
AG23	BK3_IO40		206
AH23	BK3_IO41		206
AJ23	BK3_IO42		207
GND	GND (Bank 3)		
AK23	BK3_IO43		207
GND	GND		
VCC	VCC		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
GND	GND		
VCC	VCC		
AF23	BK3_IO44		209
AE23	BK3_IO45		209
AJ24	BK3_IO46		212
VCCO3	VCCO3		
AK24	BK3_IO47		212
AH24	BK3_IO48		213
AG24	BK3_IO49	VREF3	213
AJ25	BK3_IO50		220
GND	GND (Bank 3)		
AK25	BK3_IO51		220
AF24	BK3_IO52		221
AE24	BK3_IO53		221
AK26	BK3_IO54		222
VCCO3	VCCO3		
AJ26	BK3_IO55		222
AH25	BK3_IO56		225
AG25	BK3_IO57		225
AK27	BK3_IO58		226
GND	GND (Bank 3)		
AJ27	BK3_IO59		226
AG26	BK3_IO60		227
AH26	BK3_IO61		227
VCCO3	VCCO3		
AK28	RESET		
AJ28	DXP		
AH27	DXN		
VCCO4	VCCO4		
AG28	BK4_IO0		228
AF27	BK4_IO1		228
AF28	BK4_IO2		229
GND	GND (Bank 4)		
AE26	BK4_IO3		229
AE27	BK4_IO4		230
AE28	BK4_IO5		230
AH30	BK4_IO6	HSI5A_SINN	233
VCCO4	VCCO4		
AH29	BK4_IO7	HSI5A_SINP	233
AD25	BK4_IO8		234
AD26	BK4_IO9		234
AG29	BK4_IO10	HSI5A_SOUTN	235
GND	GND (Bank 4)		
AG30	BK4_IO11	HSI5A_SOUTP	235

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
AD27	BK4_IO12	VREF4	236
AD28	BK4_IO13		236
AF29	BK4_IO14	HSI5B_SINN	237
VCCO4	VCCO4		
AF30	BK4_IO15	HSI5B_SINP	237
AC25	BK4_IO16		238
AC26	BK4_IO17		238
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AE29	BK4_IO18	HSI5B_SOUTN	239
GND	GND (Bank 4)		
AE30	BK4_IO19	HSI5B_SOUTP	239
AC28	BK4_IO20		240
AC27	BK4_IO21		240
AD29	BK4_IO22	HSI6A_SINN	241
VCCO4	VCCO4		
AD30	BK4_IO23	HSI6A_SINP	241
AB24	BK4_IO24		242
AB25	BK4_IO25		242
AC29	BK4_IO26	HSI6A_SOUTN	243
GND	GND (Bank 4)		
AC30	BK4_IO27	HSI6A_SOUTP	243
AB27	BK4_IO28		244
AB26	BK4_IO29		244
AB30	BK4_IO30	HSI6B_SINN	245
VCCO4	VCCO4		
AB29	BK4_IO31	HSI6B_SINP	245
AA26	BK4_IO32		246
AA27	BK4_IO33		246
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
AA30	BK4_IO34	HSI6B_SOUTN	247
GND	GND (Bank 4)		
AA29	BK4_IO35	HSI6B_SOUTP	247
Y25	BK4_IO36		248
Y26	BK4_IO37		248
Y28	BK4_IO38		265
VCCO4	VCCO4		
Y27	BK4_IO39		265
W25	BK4_IO40		266

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
W26	BK4_IO41		266
W27	BK4_IO42		267
GND	GND (Bank 4)		
W28	BK4_IO43		267
V24	BK4_IO44		268
V25	BK4_IO45		268
Y29	BK4_IO46		269
VCCO4	VCCO4		
Y30	BK4_IO47		269
V27	BK4_IO48	PLL_RST4	270
V28	BK4_IO49	PLL_RST5	270
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
W29	BK4_IO50		271
GND	GND (Bank 4)		
W30	BK4_IO51		271
U25	BK4_IO52		272
U26	BK4_IO53		272
V29	BK4_IO54	SS_CLKIN1N	281
VCCO4	VCCO4		
V30	BK4_IO55	SS_CLKIN1P	281
U28	BK4_IO56	PLL_FBK4	282
U27	BK4_IO57	PLL_FBK5	282
U29	BK4_IO58	SS_CLKOUT1N	283
GND	GND (Bank 4)		
U30	BK4_IO59	SS_CLKOUT1P	283
T30	BK4_IO60	CLK_OUT4	284
VCCO4	VCCO4		
T29	BK4_IO61	CLK_OUT5	284
GND	GND (Bank 4)		
T28	GCLK4		
T27	GCLK5		
T26	VCCP1		
R28	GNDP1		
R27	GCLK6		
R26	GCLK7		
GND	GND (Bank 5)		
R29	BK5_IO0	CLK_OUT6	285
VCCO5	VCCO5		
R30	BK5_IO1	CLK_OUT7	285
P30	BK5_IO2	PLL_FBK6	286
GND	GND (Bank 5)		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
P29	BK5_IO3	PLL_FBK7	286
P27	BK5_IO4		287
P28	BK5_IO5		287
P26	BK5_IO6	PLL_RST6	288
VCCO5	VCCO5		
P25	BK5_IO7	PLL_RST7	288
N27	BK5_IO8		297
N28	BK5_IO9		297
N29	BK5_IO10	HSI7A_SINN	298
GND	GND (Bank 5)		
N30	BK5_IO11	HSI7A_SINP	298
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
N25	BK5_IO12		299
N24	BK5_IO13		299
M29	BK5_IO14	HSI7A_SOUTN	300
VCCO5	VCCO5		
M30	BK5_IO15	HSI7A_SOUTP	300
M28	BK5_IO16		301
M27	BK5_IO17		301
L30	BK5_IO18	HSI7B_SINN	302
GND	GND (Bank 5)		
L29	BK5_IO19	HSI7B_SINP	302
M26	BK5_IO20		303
M25	BK5_IO21		303
K30	BK5_IO22	HSI7B_SOUTN	304
VCCO5	VCCO5		
K29	BK5_IO23	HSI7B_SOUTP	304
L28	BK5_IO24		321
L27	BK5_IO25		321
L26	BK5_IO26	HSI8A_SINN	322
GND	GND (Bank 5)		
L25	BK5_IO27	HSI8A_SINP	322
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
K27	BK5_IO28		323
K26	BK5_IO29		323
J30	BK5_IO30	HSI8A_SOUTN	324
VCCO5	VCCO5		
J29	BK5_IO31	HSI8A_SOUTP	324

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
J26	BK5_IO32		325
J27	BK5_IO33		325
H30	BK5_IO34	HSI8B_SINN	326
GND	GND (Bank 5)		
H29	BK5_IO35	HSI8B_SINP	326
J25	BK5_IO36		327
J24	BK5_IO37		327
G30	BK5_IO38	HSI8B_SOUTN	328
VCCO5	VCCO5		
G29	BK5_IO39	HSI8B_SOUTP	328
H27	BK5_IO40		329
H28	BK5_IO41		329
F30	BK5_IO42	HSI9A_SINN	330
GND	GND (Bank 5)		
F29	BK5_IO43	HSI9A_SINP	330
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
G27	BK5_IO44		331
G28	BK5_IO45		331
E30	BK5_IO46	HSI9A_SOUTN	332
VCCO5	VCCO5		
E29	BK5_IO47	HSI9A_SOUTP	332
H26	BK5_IO48		333
H25	BK5_IO49	VREF5	333
D30	BK5_IO50	HSI9B_SINN	334
GND	GND (Bank 5)		
D29	BK5_IO51	HSI9B_SINP	334
F28	BK5_IO52		335
F27	BK5_IO53		335
C30	BK5_IO54	HSI9B_SOUTN	336
VCCO5	VCCO5		
C29	BK5_IO55	HSI9B_SOUTP	336
G26	BK5_IO56		339
G25	BK5_IO57		339
F26	BK5_IO58		340
GND	GND (Bank 5)		
E28	BK5_IO59		340
E27	BK5_IO60		341
D28	BK5_IO61		341
VCCO5	VCCO5		
C27	CFG0		
B28	DONE		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
A28	PROGRAMB		
VCCO6	VCCO6		
D26	BK6_IO0	INITB	342
C26	BK6_IO1	CCLK	342
B27	BK6_IO2		343
GND	GND (Bank 6)		
A27	BK6_IO3		343
D25	BK6_IO4	CSB	345
C25	BK6_IO5	Read	345
B26	BK6_IO6		349
VCCO6	VCCO6		
A26	BK6_IO7		349
F24	BK6_IO8		350
E24	BK6_IO9		350
A25	BK6_IO10		351
GND	GND (Bank 6)		
B25	BK6_IO11		351
D24	BK6_IO12	VREF6	356
C24	BK6_IO13		356
A24	BK6_IO14		358
VCCO6	VCCO6		
B24	BK6_IO15		358
F23	BK6_IO16		359
E23	BK6_IO17		359
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
A23	BK6_IO18		362
GND	GND (Bank 6)		
B23	BK6_IO19		362
C23	BK6_IO20		363
D23	BK6_IO21		363
E22	BK6_IO22		364
VCCO6	VCCO6		
D22	BK6_IO23		364
G21	BK6_IO24		365
F21	BK6_IO25		365
B22	BK6_IO26		366
GND	GND (Bank 6)		
A22	BK6_IO27		366
E21	BK6_IO28		367
D21	BK6_IO29		367
A21	BK6_IO30		368

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
VCCO6	VCCO6		
B21	BK6_IO31		368
F20	BK6_IO32	DATA7	371
E20	BK6_IO33	DATA6	371
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
D20	BK6_IO34		372
GND	GND (Bank 6)		
C20	BK6_IO35		372
F19	BK6_IO36	DATA5	374
E19	BK6_IO37	DATA4	374
B20	BK6_IO38		375
VCCO6	VCCO6		
A20	BK6_IO39		375
D19	BK6_IO40		382
C19	BK6_IO41		382
A19	BK6_IO42		384
GND	GND (Bank 6)		
B19	BK6_IO43		384
G18	BK6_IO44		385
F18	BK6_IO45		385
A18	BK6_IO46		386
VCCO6	VCCO6		
B18	BK6_IO47		386
D18	BK6_IO48		387
C18	BK6_IO49		387
VCC	VCC		
GND	GND		
VCC	VCC		
GND	GND		
F17	BK6_IO50	DATA3	388
GND	GND (Bank 6)		
E17	BK6_IO51	DATA2	388
D17	BK6_IO52		389
C17	BK6_IO53		389
B17	BK6_IO54	DATA1	394
VCCO6	VCCO6		
A17	BK6_IO55	DATA0	394
F16	BK6_IO56		395
E16	BK6_IO57		395
D16	BK6_IO58		396
GND	GND (Bank 6)		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
C16	BK6_IO59		396
B16	BK6_IO60		397
VCCO6	VCCO6		
A16	BK6_IO61		397
GND	GND (Bank 6)		
GND	GND (Bank 7)		
A15	BK7_IO0		399
VCCO7	VCCO7		
B15	BK7_IO1		399
C15	BK7_IO2		400
GND	GND (Bank 7)		
D15	BK7_IO3		400
E15	BK7_IO4		401
F15	BK7_IO5		401
A14	BK7_IO6		403
VCCO7	VCCO7		
B14	BK7_IO7		403
C14	BK7_IO8		409
D14	BK7_IO9		409
E14	BK7_IO10		411
GND	GND (Bank 7)		
F14	BK7_IO11		411
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
C13	BK7_IO12		412
D13	BK7_IO13		412
B13	BK7_IO14		413
VCCO7	VCCO7		
A13	BK7_IO15		413
F13	BK7_IO16		415
G13	BK7_IO17		415
A12	BK7_IO18		416
GND	GND (Bank 7)		
B12	BK7_IO19		416
C12	BK7_IO20		417
D12	BK7_IO21		417
A11	BK7_IO22		424
VCCO7	VCCO7		
B11	BK7_IO23		424
E12	BK7_IO24		425
F12	BK7_IO25		425
C11	BK7_IO26		426

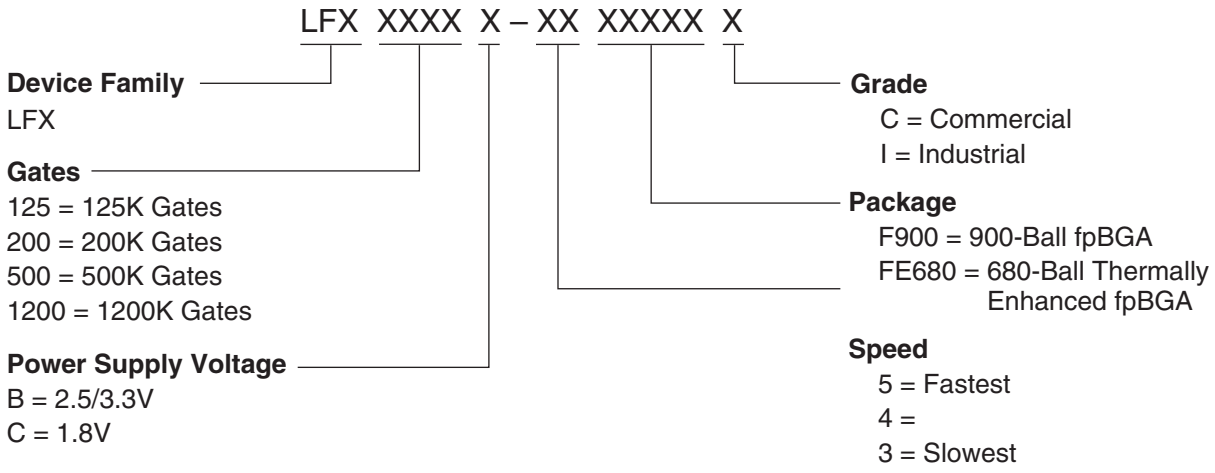
ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
GND	GND (Bank 7)		
D11	BK7_IO27		426
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
E11	BK7_IO28		427
F11	BK7_IO29		427
B10	BK7_IO30		428
VCCO7	VCCO7		
A10	BK7_IO31		428
D10	BK7_IO32		429
E10	BK7_IO33		429
A9	BK7_IO34		430
GND	GND (Bank 7)		
B9	BK7_IO35		430
F10	BK7_IO36		432
G10	BK7_IO37		432
A8	BK7_IO38		433
VCCO7	VCCO7		
B8	BK7_IO39		433
D9	BK7_IO40		434
E9	BK7_IO41		434
A7	BK7_IO42		435
GND	GND (Bank 7)		
B7	BK7_IO43		435
GND	GND		
VCC	VCC		
GND	GND		
VCC	VCC		
C8	BK7_IO44		439
D8	BK7_IO45		439
A6	BK7_IO46		441
VCCO7	VCCO7		
B6	BK7_IO47	VREF7	441
E8	BK7_IO48		446
F8	BK7_IO49		446
C7	BK7_IO50		447
GND	GND (Bank 7)		
D7	BK7_IO51		447
E7	BK7_IO52		448
F7	BK7_IO53		448
A5	BK7_IO54		449
VCCO7	VCCO7		

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900-Ball fpBGA	Signal Name	Second Function	LVDS Pair
B5	BK7_IO55		449
C6	BK7_IO56		453
D6	BK7_IO57		453
D5	BK7_IO58		454
GND	GND (Bank 7)		
C5	BK7_IO59		454
B4	BK7_IO60		455
A4	BK7_IO61		455
VCCO7	VCCO7		
A3	TDO		
B3	VCCJ		
C4	TDI		

Part Number Description



Ordering Information

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200B-05FE680C	1200K	2.5/3.3	-5	fpBGA	680
LFX1200B-04FE680C	1200K	2.5/3.3	-4	fpBGA	680
LFX1200B-03FE680C	1200K	2.5/3.3	-3	fpBGA	680
LFX1200C-05FE680C	1200K	1.8	-5	fpBGA	680
LFX1200C-04FE680C	1200K	1.8	-4	fpBGA	680
LFX1200C-03FE680C	1200K	1.8	-3	fpBGA	680
LFX1200B-05F900C	1200K	2.5/3.3	-5	fpBGA	900
LFX1200B-04F900C	1200K	2.5/3.3	-4	fpBGA	900
LFX1200B-03F900C	1200K	2.5/3.3	-3	fpBGA	900
LFX1200C-05F900C	1200K	1.8	-5	fpBGA	900
LFX1200C-04F900C	1200K	1.8	-4	fpBGA	900
LFX1200C-03F900C	1200K	1.8	-3	fpBGA	900

Note: the ispXPGA family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LFX1200B-05FE680C) than the Industrial speed grade (i.e. LFX1200B-04FE680I).

Industrial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200B-04FE680I	1200K	2.5/3.3	-4	fpBGA	680
LFX1200B-03FE680I	1200K	2.5/3.3	-3	fpBGA	680
LFX1200B-02FE680I	1200K	2.5/3.3	-2	fpBGA	680
LFX1200C-04FE680I	1200K	1.8	-4	fpBGA	680
LFX1200C-03FE680I	1200K	1.8	-3	fpBGA	680
LFX1200C-02FE680I	1200K	1.8	-2	fpBGA	680
LFX1200B-04F900I	1200K	2.5/3.3	-4	fpBGA	900
LFX1200B-03F900I	1200K	2.5/3.3	-3	fpBGA	900
LFX1200B-02F900I	1200K	2.5/3.3	-2	fpBGA	900
LFX1200C-04F900I	1200K	1.8	-4	fpBGA	900
LFX1200C-03F900I	1200K	1.8	-3	fpBGA	900
LFX1200C-02F900I	1200K	1.8	-2	fpBGA	900

Note: the ispXPGA family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LFX1200B-05FE680C) than the Industrial speed grade (i.e. LFX1200B-04FE680I).

For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispXPGA Family:

- *ispXPGA sysMEM Memory Design and Usage Guidelines* (TN1028)
- *Lattice sysCLOCK PLL Design and Usage Guidelines* (TN1003)
- *sysIO Usage Guidelines for Lattice Devices* (TN1000)
- *sysCONFIG Usage Guide* (TN1026)
- *sysHSI Usage Guide* (TN1020)